

Digital Equipment Corporation
Maynard, Massachusetts



**Maintenance Manual
PDP-9/L
Volume II**

PDP-9/L
Maintenance Manual
Volume II

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ENGINEERING DRAWINGS

GENERAL

This volume contains a complete set of engineering drawings pertaining to the basic PDP-9/L system. A formal set of engineering drawings is also shipped with each PDP-9/L system, including those for all ordered options. Where a discrepancy exists between furnished drawings and those contained in this volume, it must be assumed that the drawings furnished with the machine are correct.

USE OF DRAWING CODES

DEC engineering drawing numbers are encoded as to drawing type, major assembly, and series. A drawing number such as BS-KD09-A-11 contains the following information: BS, block schematic type; KD09, the I/O control section of the PDP-9/L; A, the manufacturing series; 11, the eleventh drawing in the I/O control series, which happens to be the teletype control schematic. In Volume I this drawing is referred to as KD11. The complete glossary of drawing type codes is as follows:

AD	Assembly Drawing
AR	Arrangement Drawing
BD	Functional Block Diagram
BS	Block Schematics
CD	Cable Diagram
CP	Component List
CS	Circuit Schematic

FD	Flow Diagram
IC	Interface Cabling Diagram
LO	Layout Drawing
MU	Module Utilization Drawing
PL	Parts List
RS	Replacement Schematic
SP	Specification Drawing
TD	Timing Diagram
UA	Unit Assembly
WD	Wiring Diagram
WL	Wiring List

DRAWING CONVENTIONS

Block schematics are multipurpose drawings that combine signal flow, logic functions, circuit type, physical location, and other pertinent information. Individual circuits are shown in block form, using special symbols which define the circuit operation. These symbols are explained in the Logic Handbook C105.

SIGNAL MNEMONIC INDEX

All signals originating in the PDP-9/L are listed in alphanumeric order below. The origin column locates the source of each signal to the particular logic drawing.

<u>Signal</u>	<u>Origin</u>	<u>Description</u>	<u>Signal</u>	<u>Origin</u>	<u>Description</u>
0 → CMA	KC19(1)	Clear the control memory address register	ADRL	KC15	Adder link
0 → MBI	KC19(2)	Clear the memory buffer input gate	ADRL(B)		
OXEN	KD3(1)	Enable devices 0X	ADSO	KC19(2)	Address switches output gate
00XXEN	KD3(1)	Enable devices 00XX	ADSO(G)	KD7(1)	
+1	KC19(1)	Increment the ADR	AM GRANT	MC1(2)	Grant core memory access to DMA channel
1 → ACI	KC19(2)	Set the accumulator register input gate	AM STROBE	MC2	Core memory strobed for DMA channel access
+1 → CA INH	KD2(2)	Inhibit increment of DCH CA register	AM SYNC	MC1	Synchronization for DMA cycle
1 → MBI	KC19(2)	Set the memory buffer input gate	AM SYNC(1)B		
1 → PCI	KC12	Set the program counter input gate	AM SYNC BUS		
13 → CMA	KC19(1)	Set CM address to 13	AND	KC19(1)	AND instruction gate
ΔMB	KC19(2)	Change the memory buffer contents	API D	CS3	Display the optional API channel activity
A,B,C	KC10(1)	Program start timing flip-flops	API IO CLR	KD3(2)	
A BUS00-05	KC20(1)	A bus contents	API ON BUS	KD7(1)	Gate optional API activity onto I/O bus (B)
A BUS06-11	KC20(2)	A bus contents	API 0,1,2,3 RQ	KD2(2)	Request API channel break
A BUS12-17	KC20(3)	A bus contents	AR00-05	KC20(1)	Arithmetic register contents
A BUS LINK	KC15	Recirculate LINK status	AR06-11	KC20(2)	Arithmetic register contents
AC00-05	KC20(1)	Accumulator register contents	AR12-17	KC20(3)	Arithmetic register contents
AC06-11	KC20(2)	Accumulator register contents	ARD	CS3	Display the arithmetic register contents
AC12-17	KC20(3)	Accumulator register contents	ARI	KC19(2)	Arithmetic register input gate
AC D	CS3	Display the accumulator register contents	ARO	KC19(3)	Arithmetic register output gate
ACI	KC19(2)	Accumulator register input gate	ARO RESTORE	KC12	Restore the arithmetic register output gate
ACO	KC19(3)	Accumulator register output gate		KC10(2)	
AC RD	KD3(3)	Read the accumulator register contents into core memory	AROS	KC10(2)	Save the arithmetic register output gate
AC RD(B)	KC19(2)	Read the accumulator register contents into core memory	AUT INX	KC14	Increment the contents of indirectly addressed core memory register 00010-17
AC SIGN	KC15	AC00 status	AXS	KC19(2)	ADD, XOR, SAD instruction gate
ADDR SW03-17	CS3	Address switch contents	B BUS00-05	KC21(1)	B bus contents
ADOF	KC15	Add data overflow, ADD instruction and DCH add-to-memory	B BUS06-11	KC21(2)	B bus contents
ADR00-05	KC21(1)	Adder register contents	B BUS12-17	KC21(3)	B bus contents
ADR06-11	KC21(2)	Adder register contents	BK	KD3(2)	Start program break process
ADR12-17	KC21(3)	Adder register contents	BK CA	KC10(1)	CA cycle of DCH break (memory extension control)
ADR = 0 SAVE	KC15	ADRA = 0, ADRB = 0 status	BK0	KD3(3)	Break cycle counter
ADRA = 0	KC21(1)	ADR00-08 = 0	BK0(0)B		
ADRB = 0	KC21(2)	ADR09-17 = 0	BK0(1)B		
	KC21(3)		BK1		
			BK1(0)B		
			BK1(1)B	KC10(1)	
			BK SYNC	KD3(2)	Synchronize program break entry
			BS SW3-4	MC2	Core memory bank selection switches

<u>Signal</u>	<u>Origin</u>	<u>Description</u>	<u>Signal</u>	<u>Origin</u>	<u>Description</u>
CAF EN	KD3(1)	Clear all flags enable	DCH EN	KD3(1)	Enable the DCH Multiplexer W104
CAF EN(B)			DCH GRANT	KD3(1)	Grant core memory access to the DCH
CAL	KC12	CAL instruction gate	DCH GRANT P		
CI17	KC14	Initiate a carry into ADR17	DCH INX	KD3(3)	Increment the DCH WC or CA register
CJIT	KC12 KC19(3)	CAL/JMS/Interrupt Transfer gate	DCH RQ	KD2(2) KD3(2)	DCH break request
CLK	KC10(1)	Main clock pulse	DCH SYNC SAVE	KD3(2)	Save the DCH SYNC status
CLK(B)	KD3(2)		DEI	KC19(1)	Initiate the defer or execute cycle
CLK DLY'D	KD3(3)	Main clock pulse delayed 500 ns	DIGIT READ DRIVE	MC1(2)	Turn on core memory address selectors
CLL	KC13	Clear the LINK	DIGIT READ ON	MC2	Turn on DIGIT READ DRIVE, DIGIT READ SINK
CLR	KC16	Clear the +1, ACO gates, set the SAO, ARO gates	DIGIT WRITE DRIVE	MC1(2)	Turn on core memory address selectors
CLR I	KC19(2)	Clear the MBO, ACI, ARI, PCI, MQI gates	DIGIT WRITE SINK	MC1(2)	Turn on core memory address selectors
CLR PUN	KD10(1)	Clear the punch buffer and punch flag	DLY	KD3(3)	Clock pulse delayed 500 ns
CLR RDR	KD9(1)	Clear the RDR FLG, RDR 1, RDR 2 flip-flops	DONE	KC19(1)	Instruction DONE gate
CMA00-05	KC19(1)	Control memory address register contents	DONE(1)B	KD3(2)	
CM CLK	KC10(1)	Main clock pulse to control memory	DPY D	CS3	Display x, y buffers of optional 34H Display
CM CURRENT	KC16	Turn on control memory address selectors	DPY ON BUS	KD7(1)	Gate x, y buffers of optional 34H Display onto the IO Bus(B)
CMG00-07	KC17	Control memory current lines	DS00-05	KD3(1)	Device select bits
CML	KC13	Complement the LINK	DS00P-05P		
CMPL	KC13	Complement the ADR contents	EAE	KC19(1)	Optional extended arithmetic element gate
CMP00-07	KC17	Control memory current lines	EAE D	CS3	Not wired
CMSL00-35	KC17 KC18(2)	Control memory sense lines	EAE-P	KC19(1)	Optional extended arithmetic element gate
CM STROBE A,B,C,D	KC16	Strobe the control memory	EAE-R		
CM STROBE DLYD	KC16		EAE STROBE DLYD	KC16	CM STROBE delayed for optional extended arithmetic element
CONT	KC19(1)	Continue gate	END BIT 0	KC15	LINK to ADRL to AC17. Also for optional extended arithmetic element gating
CO00-05	KC21(1)	Carry out of ADR00-05	END BIT 17	KC15	Optional extended arithmetic element gating
CO06-11	KC21(2)	Carry out of ADR06-11	EXT	KC19(3)	External transfer gate (program breaks)
CO12-17	KC21(3)	Carry out of ADR12-17	EXT(1)B	KD3(3)	
DASO	KC13	Data switches output gate	FEED HOLE	KD9(2)	Reader no-tape sensor
DATA OFLO	KC15	DCH add-to-memory data overflow	FWD FD and NDX	KD10(1)	Punched tape drive power
DATA SW00-17	CS3	Data switch contents	GO DLY	KD9(1)	Reader enable delay
DB RESTORE	KD3(1)		IND CLK	KC10(1)	Gate CP register contents for display
DBR	KD3(1)	Debreak and restore the interrupted program	IN CLR	KC16	Generate CLR I
DBR(B)	KC15		INC V DCH	KD3(2)	Enter DCH or RTC WC cycle
DCH	KC19(1)				
DCH BK DLY	KD3(1)	Illuminate the DCH display indicator			

<u>Signal</u>	<u>Origin</u>	<u>Description</u>	<u>Signal</u>	<u>Origin</u>	<u>Description</u>
IND EN	KC10(1)	Enable console display selector switch	IO PWR CLR	KD3(1)	I/O power clear pulse
INC MB	KD2(2) KD3(3)	Increment the memory buffer contents	IO PWR CLR POS	KD3(1)	
IN LAST UNIT	KD11(1)	Last keyboard code unit shifted into input buffer	IO RESTART	KD3(3)	Restart control memory after manual read-in, EAE, or IOT instruction execution
INPUT IO RESTART	KD8 KD3(3)	Restart control memory after manual read-in, EAE, or IOT instruction	IO RUN(1)	KD3(1)	Computer RUN condition to I/O devices
INT RD RQ BUS	KD3(3)	Internal read request bus	IO SKIP	KD3(3)	Skip next instruction on SKIP RQ from I/O device
INT SKP RQ BUS	KD3(1) KD9(1) KD10(1) KD11(1) KD11(2)	Internal skip request bus	IO SYNC	KD3(1)	Synchronize program break entry
IO0	KD3(3)	Input/output transfer cycle counter	IO SYNC IN	KD3(2)	Synchronize program break entry
IO1			IO SYNC POS	KD3(2)	Synchronize program break entry
IO ADDR 03-17	KD2(2)	DCH and optional API channel address	IO SYNC SP	KD3(1)	Synchronize optional API break entry
IO ADDR 03(B)-17(B)	KD5		IOT	KC12	Input/output transfer gate
IO ADDR 12,16,17	KD5	Optional API channel address	IOT0002	KD3(1)	IOT command
IO ADDR D	CS3	Display DCH or optional API address	IOT0004	KD3(1)	
IO ADDR ON BUS	KD7(1)	Gate DCH or optional API address onto I/O bus (B)	IOT0102	KD9(1)	
IO BUS00-05	KC21(1)	I/O bus contents	IOT0104	KD9(1)	
IO BUS06-11	KC21(2)		IOT0204	KD10(1)	
IO BUS12-17	KC21(3)		IOT0302	KD11(1)	
IO BUS00-17	KD2(1)		IOT0404	KD11(2)	
IO BUS00(B)-08(B)	KD7(1)	I/O bus buffered	IOT3344	KD3(1)	
IO BUS09(B)-17(B)	KD7(2)		IOT(B)	KD3(1)	Input/output transfer gate
IO BUS ON	KC19(3)	ADR to I/O bus gate	IOT OR ARO	KC12	Set ARO gate for programmed output transfer
IO CLK (B)	KD3(3)	Main clock pulse	IOT PWR CLR	KD3(1)	
IO CLK POS	KD3(2)	Main clock pulse	IR00-04	KC12	Instruction register contents
IO CLR	KD3(2)	Clear PROG SY, PROG SYNC, BK	IRI	KC19(1)	Instruction register input gate
IO OFLO	KD3(2)	DCH or RTC operations completed	ISZ	KC12	ISZ instruction gate
IOP1	KD3(1) KD3(3)	Input/output pulse 1	KBD FLG	KD11(1)	Keyboard flag
IOP2	KD3(1) KD3(3)	Input/output pulse 2	KBD SEL	KD11(1)	Keyboard select
IOP4	KD3(1) KD3(3)	Input/output pulse 4	KBD SEL(B)		
IOP1P	KD3(3)	Input/output pulse 1	KCT	CS3	CONTINUE key
IOP2P	KD3(3)	Input/output pulse 2	KCT(B)	KC10(1)	
IOP4P	KD3(3)	Input/output pulse 4	KDN	CS3	DEPOSIT NEXT key
			KDP	CS3	DEPOSIT key
			KDPDN	KC10(1)	DEPOSIT/DEPOSIT NEXT key
			KDPDN V RI	KC19(3)	DEPOSIT/DEPOSIT NEXT key or READ-IN key
			KDPM	CS5	DEPOSIT key (maintenance)
			KEY	KC19(2)	Key gate
			KEY BUS	KC10(1)	Key bus
			KEY BUS(B)		
			KEY DLY	KC10(1)	Delay key-activated RUN condition

<u>Signal</u>	<u>Origin</u>	<u>Description</u>	<u>Signal</u>	<u>Origin</u>	<u>Description</u>
KEY INIT POS	KC10(1)	Initiate key operations	MB00-05	KC21(1)	Memory buffer register contents
KEY \wedge KDPDN	KC13		MB06-11	KC21(2)	
KEN	CS3	EXAMINE NEXT key	MB12-17	KC21(3)	
KEYS	CS5		MBI	KC19(2)	Memory buffer input gate
KEX	CS3	EXAMINE key	MBI(1)B	KC28	
KIO	CS3	I/O RESET key	MBO	KC19(3)	Memory buffer output gate
KIOA3, A4, A5	KC10(1)	Key process address to control memory	MBS00-17	MC3	Core memory input mixer bits
KMT	CS5	Key (maintenance)	MEM DONE	MC1(2)	Core memory cycle done
KRI	CS3	READ-IN mode key	MEM DONE(1)B		
KSP	CS3	STOP key	MEM STROBE	MC2	Core memory strobed for CP access
KST	CS3	START key	MEM STROBE(B)	KC28	
KXDM	CS5	EXAMINE/DEPOSIT key (maintenance)	MK	CS5	
LAR	KC15	Arithmetic register link	MODE	MC1(2)	Core memory access mode
LI	KC19(1)	LINK input gate	MQ00-05	KC20(1)	Optional multiplier/quotient register contents
LINK	KC15	Accumulator register link	MQ06-11	KC20(2)	
LIO	KC13	Load I/O data onto I/O bus	MQ12-17	KC20(3)	
LOCK	CS5	Lock the console controls	MQ D	CS3	Display the optional multiplier/quotient register contents
LOT	KC12	LAW/OPR/IOT instruction gate	MQI	KC19(2)	Optional multiplier/quotient input gate
MA05-13	MC1(1)	Memory address register contents	MQO	KC19(3)	Optional multiplier/quotient output gate
MA14A-17A			NDX	KD10(1)	Punch the tape feed holes
MA14B-17B			NOSH	KC13	NO SHIFT gate
MA06(0) \wedge MA07(0)	MC1(1)	Memory address register bits decoded for address selection	O BUS00-05	KC20(1)	O bus contents
			O BUS06-11	KC20(2)	
			O BUS12-17	KC20(3)	
			O BUS00-17	KC22	
MA06(0) \wedge MA07(1)			O BUS L	KC15	LINK status to optional EAE
MA06(1) \wedge MA07(0)			OFLO	KC14	DCH, RTC word count overflow
MA06(1) \wedge MA07(1)			OFLO	KC15	ADD instruction overflow
MA10(0) \wedge MA11(0)			OP	KC12	OPR instruction gate
MA10(0) \wedge MA11(1)			OR ACI	KC12	Set the ACI gate for programmed input transfer
MA10(1) \wedge MA11(0)			OR MBO	KC12	Set the MBO gate for LAW instruction
MA10(1) \wedge MA11(1)			PB10-17	KD10(1)	Punch buffer contents
WR(1) \wedge MA05(1)			PC05	KC20(1)	Program counter contents
\vee WW(1) \wedge MA05(0)			PC06-17	KC20(2)	
WR(1) \wedge MA05(0)			PC012-17	KC20(3)	
\vee WR(1) \wedge MA05(1)			PC D	CS3	Display the program counter contents
MA JAM DIGIT	MC1(1)	Strobe address into memory address register	PCI	KC19(2)	Program counter input gate
MA JAM PAR			PCO	KC19(3)	Program counter output gate
MA JAM WORD			PCO RESTORE	KC10(2)	Restore the PCO gate
MAS03-04	MC2	Memory address bits decoded for expanded memory			

<u>Signal</u>	<u>Origin</u>	<u>Description</u>	<u>Signal</u>	<u>Origin</u>	<u>Description</u>
PCOS	KC10(2)	Save the PCO gate	RD IO BUS	KD7(1)	
PIE	KD3(2)	Program interrupt enable	RDR 1	KD9(1)	Read first line of tape into reader buffer
PIE(0)	KD3(2)	Program interrupt disable	RDR 2	KD9(1)	Read second line of tape into reader buffer
PK CLR	KC10(1)	Power and key clear pulse	RDR A	KD9(1)	Reader line index count
PK CLR(B)	MC2		RDR A(0)B	KD9(2)	
POST CLK	MC2	Main clock delayed/strobe the MODE flip-flop	RDR A(1)B	KD9(2)	
PRE-STROBE	MC2	Generate MEM STROBE, STROBE SAL, STROBE SAR	RDR ALPHA	KD9(1)	Reader alpha mode
PRE-WRITE OFF	MC2	Set MEM DONE, issue AM GRANT	RDR B	KD9(1)	Reader line index count
PROG INT RQ	KD2(1)	Program interrupt request	RDR B(0)B	KD9(2)	
	KD3(2)		RDR B(1)B	KD9(2)	
	KD9(2)		RDR CLK	KD9(1)	Reader clock pulse
	KD10(1)		RDR CLK EN	KD9(1)	Reader clock enable
	KD11(1)		RDR COUNT	KD9(1)	Reader line index count
	KD11(2)		RDR D	CS3	Display the reader buffer contents
PROG SY	KD3(2)	Synchronize program interrupt entry	RDR FEED	KD9(2)	Feed tape manually without reading
PROG SY(1)B			RDR FLG	KD9(1)	Reader flag
PROG SYNC			RDR FLG(B)	KD8	
PROG SYNC(1)B			RDR GO	KD9(1)	Enable reader clock
PUN	KD10(1)	Punch mechanism operating	RDR INDEX	KD9(1)	Reader clock pulses
PUN ACT	KD10(1)	Actuate punch mechanism	RDR NO TAPE	KD9(1)	Reader out of tape
PUN FEED	KD10(2)	Punch feed holes manually	RDR ON BUS	KD7(1)	Gate reader buffer contents onto I/O bus (B)
PUN FLG	KD10(1)	Punch flag	RDR PWR	KD9(1)	Reader power
PUN HOLE 1-8	KD10(1)	Punch buffer bits to punch solenoids	RDR RUN	KD9(1)	Generate RUN
PUN LINE	KD10(1)	Enable punch solenoid drivers	RDR SEL	KD9(1)	Reader select
PUN NO TAPE	KD10(1)	Punch out of tape	RDR SEL(B)		
PUN PWR	KD10(1)	Punch power	RD RQ	KD2(1)	Read request from I/O device
PUN PWR ON	KD10(1)	Punch power on	RD RQ(B)	KD3(3)	
PUN SEL	KD10(1)	Punch select	RD START RQ	KC10(1)	Read manually entered tape word into core memory
PUN SPD	KD10(1)	Punch motor up to speed	RD STATUS	KD11(1)	Read teletype status
PUN SYNC	KD10(2)	Punch motor in punching position	R12(1)B	KD8	Manually entered tape word count
PV	KC12	Memory protection violation	RQ MBI	KC19(2)	Turn on memory buffer input gate
PWR(B)	KD9(1)	Reader power on	RSB	KD8	Select reader binary mode
PWR CLR POS	KC10(1)	Power clear pulse	RUN	KD9(1)	Set RDR GO
RB00-17	KD9(2)	Reader buffer contents	RUN	KC10(1)	Computer program started
RD HOLE 1(B)-7(B)	KD9(2)	Punched tape contents	RUN(1)B		
RD HOLE 7(C)	KD9(2)	Punched hole 7	RUN(0)	KC10(1)	Computer program stop
RD HOLE 8(B)	KD9(2)	Punched hole 8	SA00-17	MC6	Sense amplifier contents
RD HOLE 8P V ALPHA	KD9(2)	Reader binary or alpha mode	SAO	KC19(3)	Sense amplifier output gate
			SAO(0)B	KC15	

<u>Signal</u>	<u>Origin</u>	<u>Description</u>
SD00-01 SD00P-01P	KD3(1)	Special device select bits
SEN SEN(1)B	KC10(2) KC10(1)	Computer RUN sensor
SHIFT	KC15	Shift ADR contents enable
SHL1	KC13	Shift ADR contents left one position
SHL2	KC13	Shift ADR contents left two positions
SHR1	KC13	Shift ADR contents right one position
SHR2	KC13	Shift ADR contents right two positions
SKIP	KC14	Skip next instruction gate
SKIP RQ	KD2(1)	Skip request from I/O device
SKPI	KC19(1)	Skip input gate
SM	KC19(2)	Start memory gate
SPEED 2,3,4	CS3	Repeat speed selections
SPEED WIPER	CS3	Repeat speed switch wiper
STATUS D	CS3	Display the I/O device status bits
STATUS ON BUS	KD7(1)	Gate the I/O device status bits onto I/O bus (B)
STOP DLY	KD9(1)	Decelerate the reader motor
<u>STOP DLY</u>	KD9(1)	Permit reader motor to restart
STOP DLY POS	KD9(1)	Disable reader clock
STROBE DLYD	KC16	Control memory strobe delayed
STROBE SAL	MC2	Strobe the left hand sense amplifiers
STROBE SAR	MC2	Strobe the right hand sense amplifiers
SW EXD	CS3	Optional memory extend mode switch
SW SGL INST	CS3	Single instruction switch
SW PARITY	CS3	Optional memory parity switch
SW PRTCT	CS3	Optional memory protect switch
SW REPT	CS3	Repeat switch
SUB	KC19(1)	Subtract gate
SYNC CLK	MC2	Set AM SYNC if AM RQ is present
TAPE	KD10(2)	Punch out of tape
TI	KC19(1)	Test for indirect address gate
T-PRNTR FLG	KD11(2)	Teleprinter flag
T-PRNTR SEL T-PRNTR SEL(B)	KD11(2)	Select teleprinter
TT100-07	KD11(1)	Teletype input buffer contents

<u>Signal</u>	<u>Origin</u>	<u>Description</u>
TTI CLK	KD11(1)	Teletype input clock
TTI D	CS3	Display the teletype input buffer contents
TTI FULL	KD11(1)	Teletype input buffer is full
TTI INITIALIZE	KD11(1)	Initialize teletype input buffer and controls
TTI LOAD	KD11(1)	Load the teletype input buffer
TT IN ACT	KD11(1)	Teletype input circuits active
TTI ON BUS	KD7(1)	Gate teletype input buffer contents onto I/O bus (B)
TT KBD IN TT KBD IN(B)	KD11(1)	Teletype keyboard input
TT LINE	KD11(2)	Actuate teleprinter to generate space or mark
TTO00-07	KD11(2)	Teletype output buffer contents
TTO CLK	KD11(2)	Teletype output clock
TTO EN	KD11(2)	Teletype output enable
TTO EQ	KD11(2)	All teletype output buffer bits serially shifted into teleprinter
TTO LOAD	KD11(2)	Load the teletype output buffer
TTO OUT ACT	KD11(2)	Teletype output circuits active
TT RDR RUN	KD11(1)	Release teleprinter magnet to generate marks and spaces
TTO START	KD11(2)	Start teletype output operations
TTO STOP	KD11(2)	Stop teletype output operations
WORD READ	MC1(2)	Turn on core memory address selectors
WORD READ ON	MC2	Turn on WORD READ
WORD WRITE	MC1(2)	Turn on core memory address selectors
WRITE OFF	MC2	Turn off core memory address selectors
WRITE ON	MC2	Turn on DIGIT WRITE DRIVE, DIGIT WRITE SINK
WR RQ	KD2(2) DK3(3)	Write request from I/O device
<u>WR RQ(B)</u>	KD3(2)	

9/L SYSTEM

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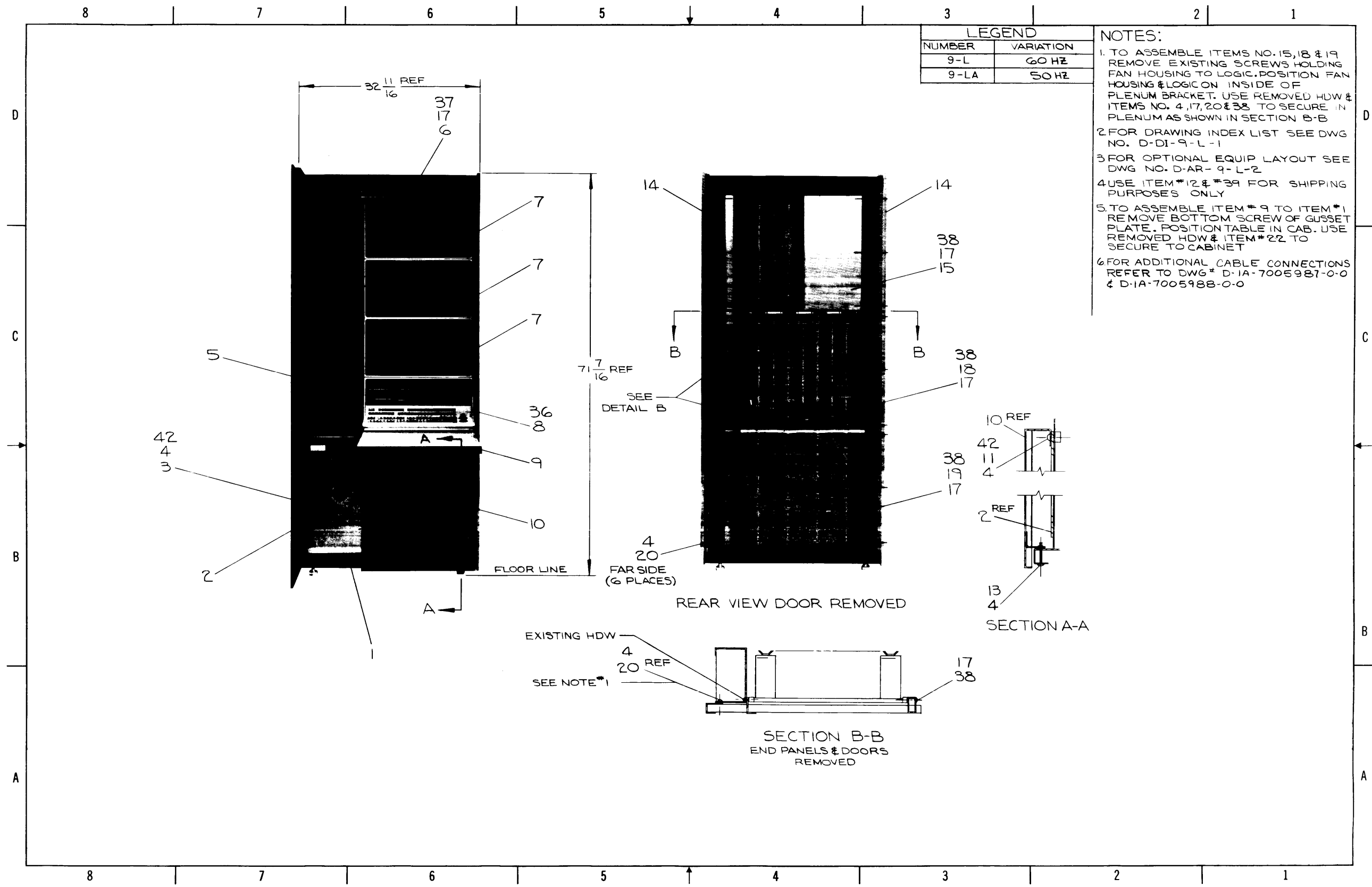
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DIGITALEQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION					
1	E-AD-7005870-0-0	CABINET FRAME 9L						
2	D-UA-712-0-0	POWER SYPPLY 712	9-L					
2	D-UA-712-A-0	POWER SUPPLY 712-A	1					
3	9006073-3	PHL HD TRUSS #10-32 x 1/2	1					
4	9007651	WASH EXT TOOTH #10	25					
5	D-UA-H951-TA-0	H951-TA NARROW DOOR	23					
6	D-IA-7406731-0-0	LOGO PDP-9L	1					
7	D-UA-H950-Q-0	H950-Q 19" COVER PANEL 10 1/2"	1					
8	E-AD-7005875-0-0	9L CONSOLE ASSY	3					
9	D-AD-7005859-0-0	TABLE ASSEMBLY	1					
10	D-IA-7406723-0-0	KICK PANEL	1					
11	9006074-3	PHL HD TRUSS #10-32 x 5/8	2					
12	9006565	NUT KEPS #10-32 SST	3					
13	9006082-3	PHL HD TRUSS #10-32 x 2 1/4	2					
14	D-UA-H952-A-0	END PANEL H952-A	2					
15	D-UA-MC71-A-0	4K BASIC MEMORY	1					
16	9007033	TIE WRAP #SSC-2-B (PANDUIT)	A/R	A/R				
17	9006724	WASH EXT TOOTH 1/4	11	11				
18	D-UA-KC09-C-0	CENTRAL PROCESSOR ASSY KC09-C	1	1				
19	D-UA-KD09-C-0	I/O SECTION ASSY KD09-C	1	1				
20	9006075-1	PHL HD PAN #10-32 x 3/4 SST	6	6				
21	D-UA-H951-B-0	30" FULL DOOR ASSY	1	1				

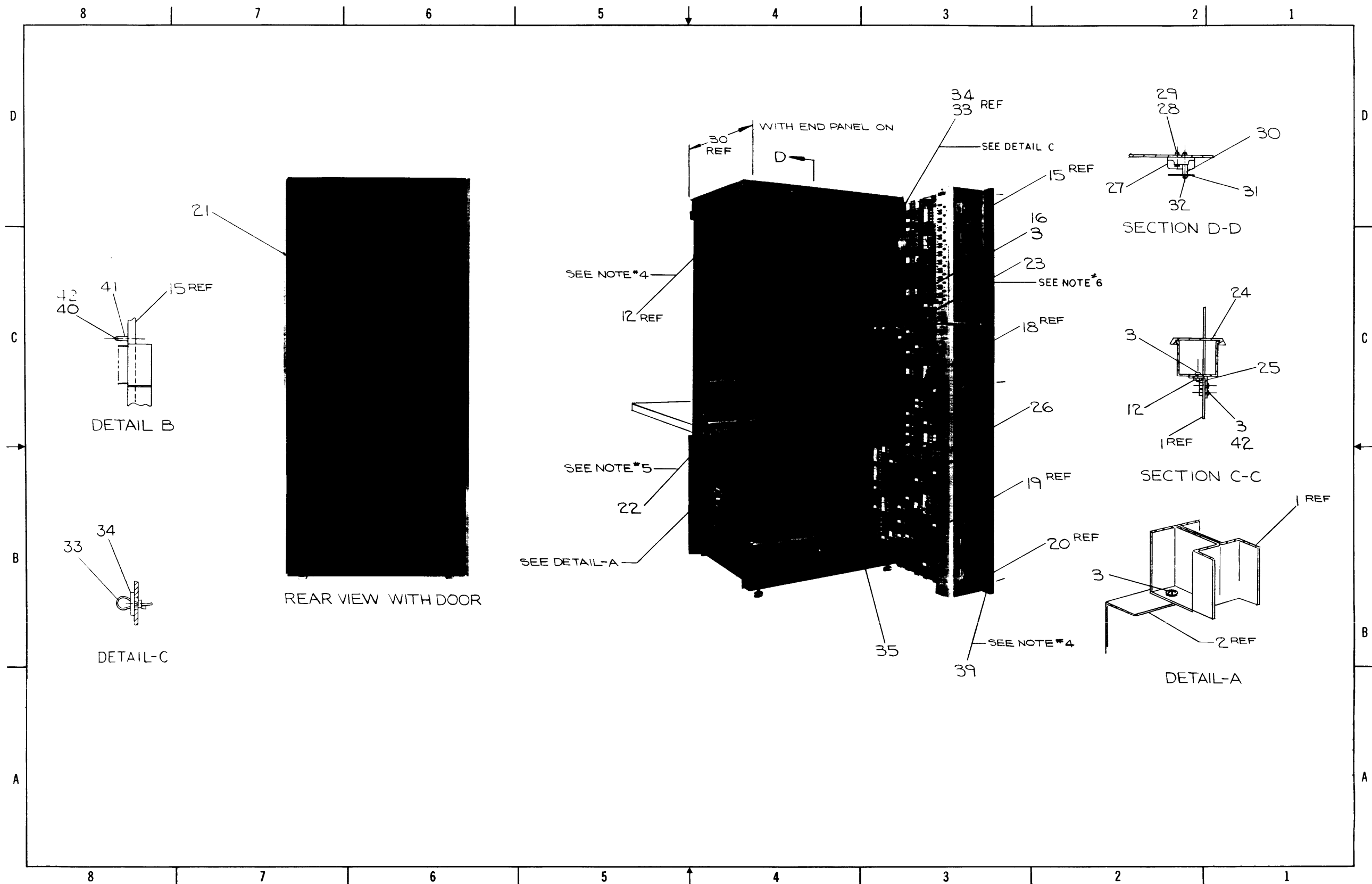
DIGITALEQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION					
22	9006056-1	PHL HD PAN 1/4-20 x 1/2 SST	2	2				
23	C-AD-7005968-0-0	CABLE SET 9L	1	1				
24	C-MD-7406734-0-0	DUCT CABLE	1	1				
25	D-MD-7406732-0-0	SUPPORT DUCT	1	1				
26	D-IC-9-L-3	POWER WIRING 9L	1	1				
27	9006902	TERM STRIP 4-541 CINCH JONES	1	1				
28	9006026-1	PHL HD PAN 6-32 x 3/4 SST	4	4				
29	9006560	NUT KEPS HEX #6-32 SST	2	2				
30	9006851	SPACER 1/4 AF x 1/2 #6-32 AL	2	2				
31	B-MD-7404721-0-0	PROTECTION CONVER 541 (4 TERM)	1	1				
32	9006020-1	PHL HD PAN #6-32 x 1/4	2	2				
33	9007032	TIE WRAP #SST-2-B (PANDUIT)	A/R	A/R				
34	9006712	WASH .250 I.D. X.375 O.D. X.032THK	A/R	A/R				
35	9107240	HELITUBE 1/4 O.D.	A/R	A/R				
36	9006071-2	PHL HD FLAT #10-32 x 3/8	4	4				
37	9006065-1	SCR PHL HD PAN 1/4-20 x 2 1/4 LG	2	2				
38	9006062-1	SCR PHL HD PAN 1/4-20 x 1 1/2	9	9				
39	9006079-3	SCR PHL HD TRUSS #10-32 x 1 1/2	3	3				
40	9006046-1	SCR PHL HD PAN #8-32 x 1-3/4 LG	2	2				
41		SPACER 3/8 AF x 1-1/2 LG. - #10 HOLE	2	2				
42	9007786	SPEED NUT 10-32 TINNEMAN	20	20				
43	9006634	WASH INT TOOTH # 8	2	2				



LEGEND	
NUMBER	VARIATION
9-L	60 HZ
9-LA	50 HZ

- NOTES:
1. TO ASSEMBLE ITEMS NO. 15, 18 & 19 REMOVE EXISTING SCREWS HOLDING FAN HOUSING TO LOGIC. POSITION FAN HOUSING & LOGIC ON INSIDE OF PLENUM BRACKET. USE REMOVED HDW & ITEMS NO. 4, 17, 20 & 38 TO SECURE IN PLENUM AS SHOWN IN SECTION B-B
 2. FOR DRAWING INDEX LIST SEE DWG NO. D-DI-9-L-1
 3. FOR OPTIONAL EQUIP LAYOUT SEE DWG NO. D-AR-9-L-2
 4. USE ITEM #12 & #39 FOR SHIPPING PURPOSES ONLY
 5. TO ASSEMBLE ITEM #9 TO ITEM #1 REMOVE BOTTOM SCREW OF GUSSET PLATE. POSITION TABLE IN CAB. USE REMOVED HDW & ITEM #22 TO SECURE TO CABINET
 6. FOR ADDITIONAL CABLE CONNECTIONS REFER TO DWG # D-1A-7005987-0-0 & D-1A-7005988-0-0

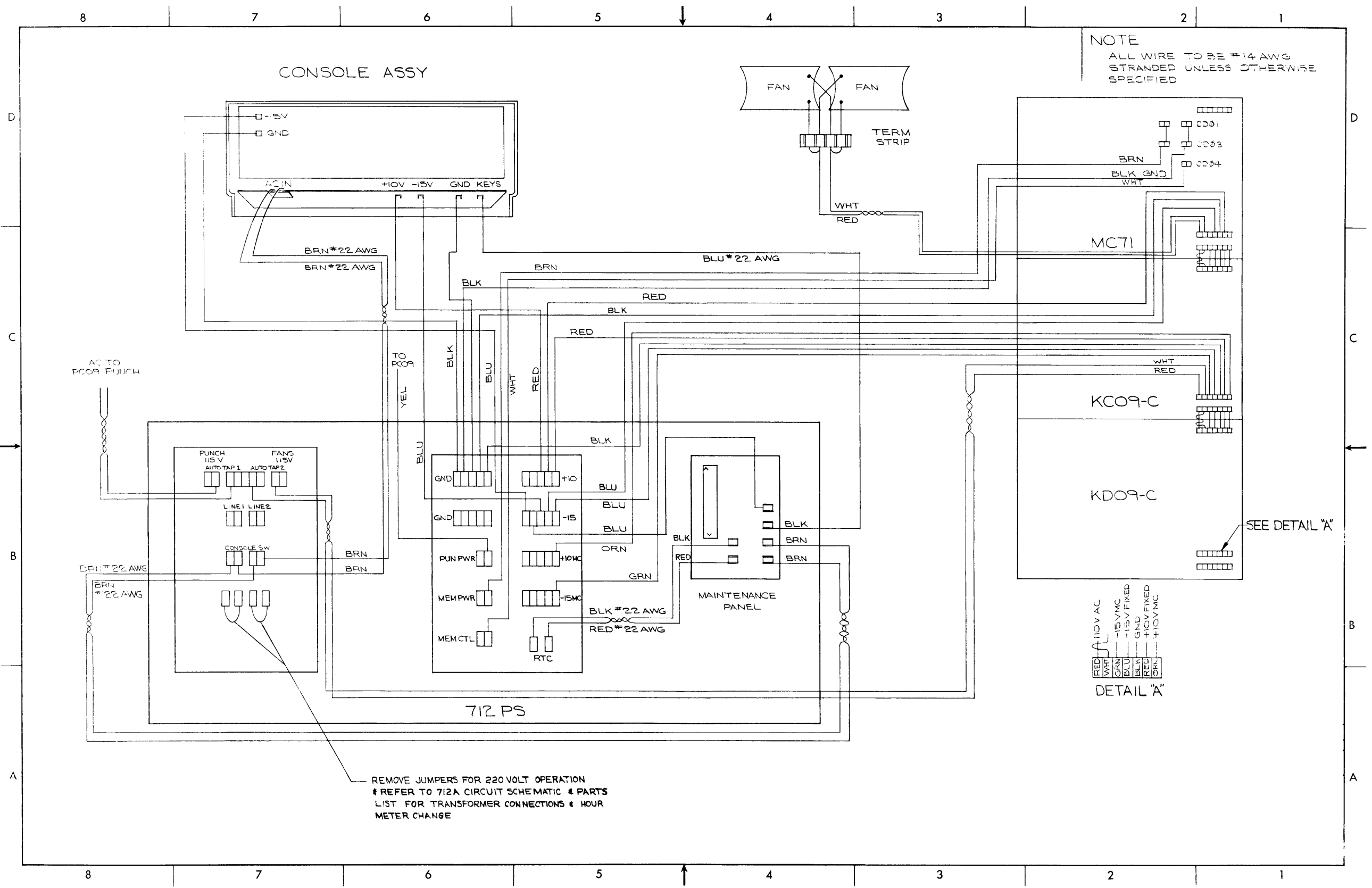


D-UA-9-L-0 PDP-9/L Assembly (Sheet 2)

ITEM NO.	PART NO.	LENGTH	CONN TYPE	TO LOCATION	CONN TYPE	TO LOCATION
1	7405552-5	6	W031	CPD40	W031	IO D01
				CPD39		IO D09
				CPE40		IO E01
				CPE39		IO E02
				CPF40		IO F01
				CPF39		IO F02
				CPF38		IO F03
				CPH40		IO H01
1	7405552-5		W031	CPH39	W031	IO H02
2	7405554-15		W034	CPJ40	W034	IO J01
2	7405554-15		W034	CPJ39	W034	IO J02
1	7405552-5	6	W031	CPJ38	W031	IO J03
3	7405553-15	49	W033	712 PS	W033	IO A06
4	7405553-16	61	W033	READER	W033	IO A17
4	7405553-16	61	W033	PUNCH	W033	IO A21

} OPTIONAL

2	W033 TO W033 CABLE (61")	C1A-7405553-16-0	4
1	W033 TO W033 CABLE (49")	C1A-7405553-15-0	3
2	W034 TO W034 CABLE (6")	C1A-7405554-15-0	2
10	W031 TO W031 CABLE (6")	C1A-7405552-5-0	1
QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			

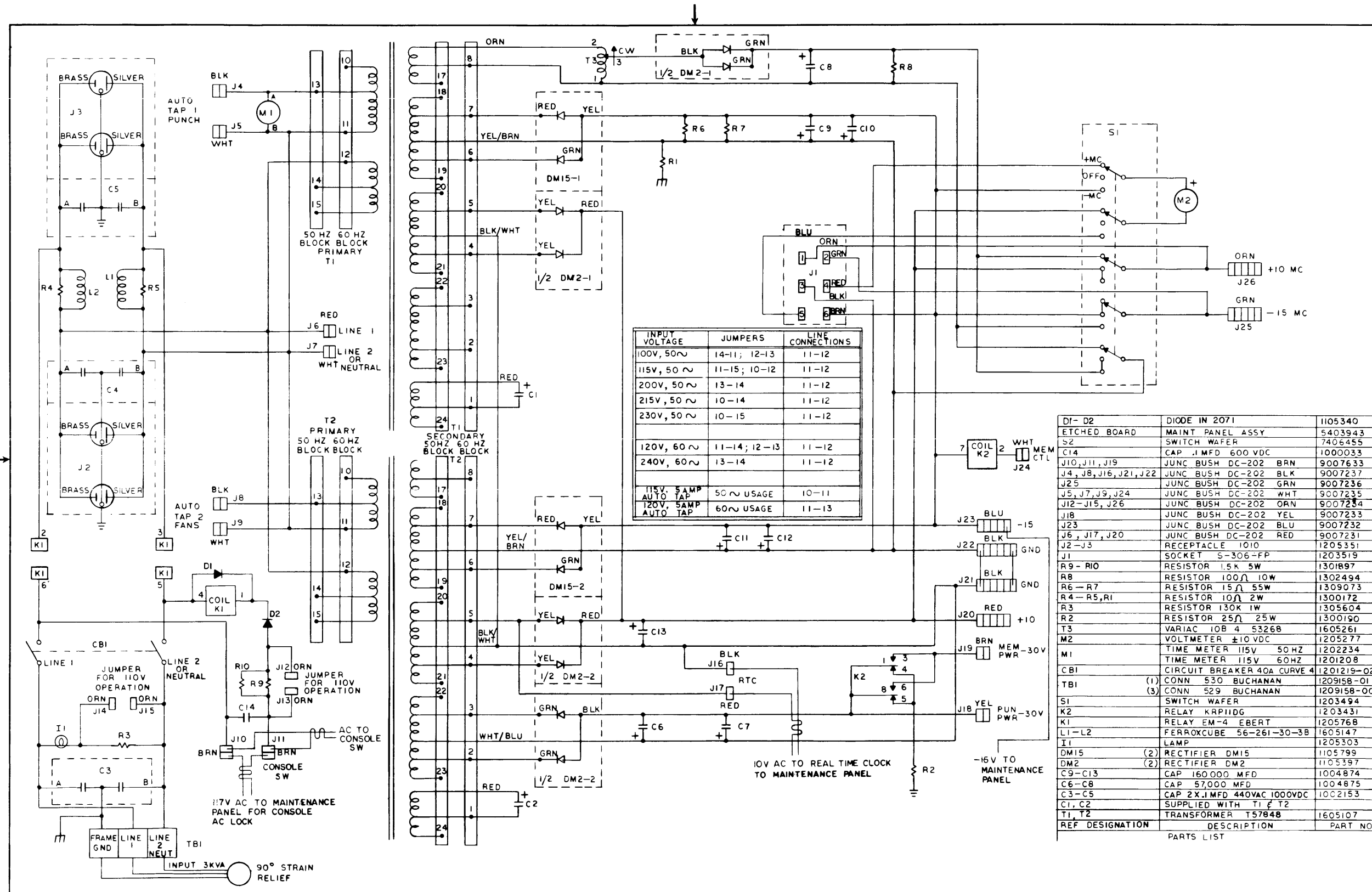


NOTE
ALL WIRE TO BE #14 AWG
STRANDED UNLESS OTHERWISE
SPECIFIED

DETAIL "A"
 RED +110V AC
 WHT -15V MC
 GRN -15V MC
 BLU -15V FIXED
 BLK -15V FIXED
 WHT GND
 RED +10V FIXED
 ORN +10V MC
 GRN +10V MC

REMOVE JUMPERS FOR 220 VOLT OPERATION
 # REFER TO 712A CIRCUIT SCHEMATIC & PARTS
 LIST FOR TRANSFORMER CONNECTIONS & HOUR
 METER CHANGE

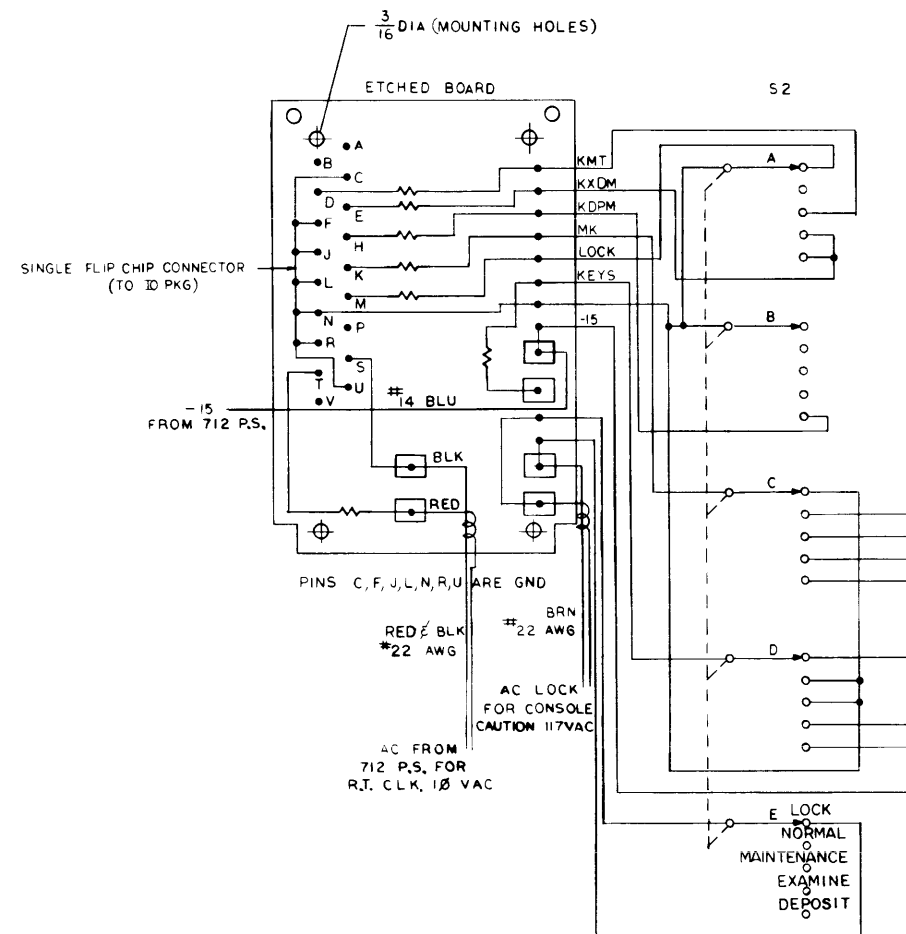
D-IC-9-L-3 Power Wiring



DI- D2	DIODE IN 2071	1105340
ETCHED BOARD	MAINT PANEL ASSY	5403943
S2	SWITCH WAFER	7406455
C14	CAP .1 MFD 600 VDC	1000033
J10, J11, J19	JUNC BUSH DC-202 BRN	9007633
J4, J8, J16, J21, J22	JUNC BUSH DC-202 BLK	9007237
J25	JUNC BUSH DC-202 GRN	9007236
J5, J7, J9, J24	JUNC BUSH DC-202 WHT	9007235
J12- J15, J26	JUNC BUSH DC-202 ORN	9007234
J18	JUNC BUSH DC-202 YEL	9007233
J23	JUNC BUSH DC-202 BLU	9007232
J6, J17, J20	JUNC BUSH DC-202 RED	9007231
J2- J3	RECEPTACLE 1010	1205351
J1	SOCKET S-306-FP	1203519
R9- R10	RESISTOR 1.5K 5W	1301897
R8	RESISTOR 100Ω 10W	1302494
R6- R7	RESISTOR 15Ω 55W	1309073
R4- R5, R1	RESISTOR 10Ω 2W	1300172
R3	RESISTOR 130K 1W	1305604
R2	RESISTOR 25Ω 25W	1300190
T3	VARIAC 10B 4 5326B	1605261
M2	VOLTMETER ±10 VDC	1205277
M1	TIME METER 115V 50 HZ	1202234
	TIME METER 115V 60 HZ	1201208
CBI	CIRCUIT BREAKER 40A CURVE 4	1201219-02
TBI	(1) CONN 530 BUCHANAN	1209158-01
	(3) CONN 529 BUCHANAN	1209158-00
S1	SWITCH WAFER	1203494
K2	RELAY KRPI1DG	1203431
K1	RELAY EM-4 EBERT	1205768
L1- L2	FERROXCUBE 56-261-30-3B	1605147
I1	LAMP	1205303
DM15	(2) RECTIFIER DM15	1105799
DM2	(2) RECTIFIER DM2	1105397
C9- C13	CAP 160 000 MFD	1004874
C6- C8	CAP 57,000 MFD	1004875
C3- C5	CAP 2X.1 MFD 440VAC 1000VDC	1002153
C1, C2	SUPPLIED WITH T1 & T2	
T1, T2	TRANSFORMER T57B4B	1605107
REF DESIGNATION	DESCRIPTION	PART NO

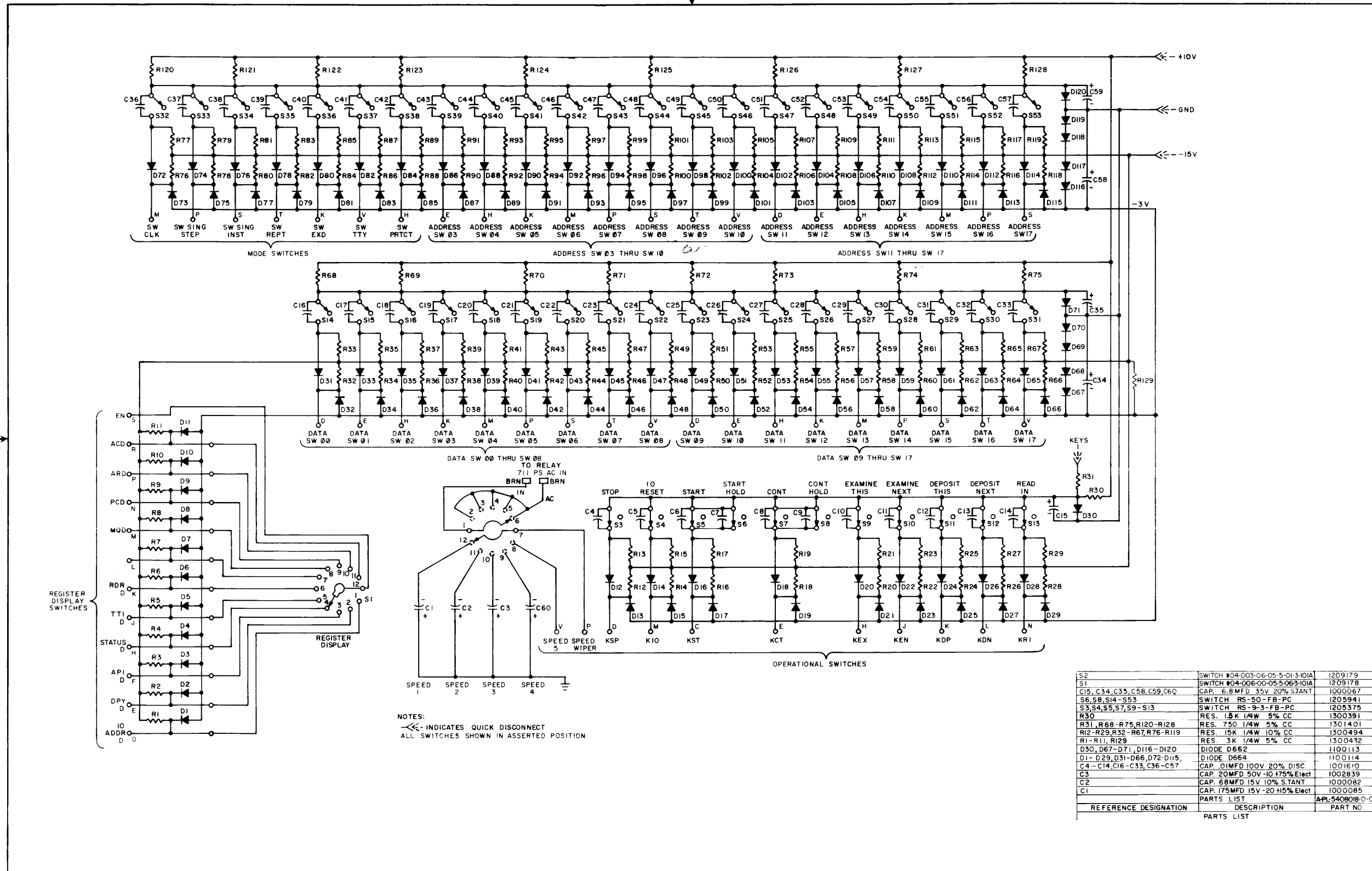
PARTS LIST

D-IC-712-0-1 Power Supply 712 (Sheet 1)

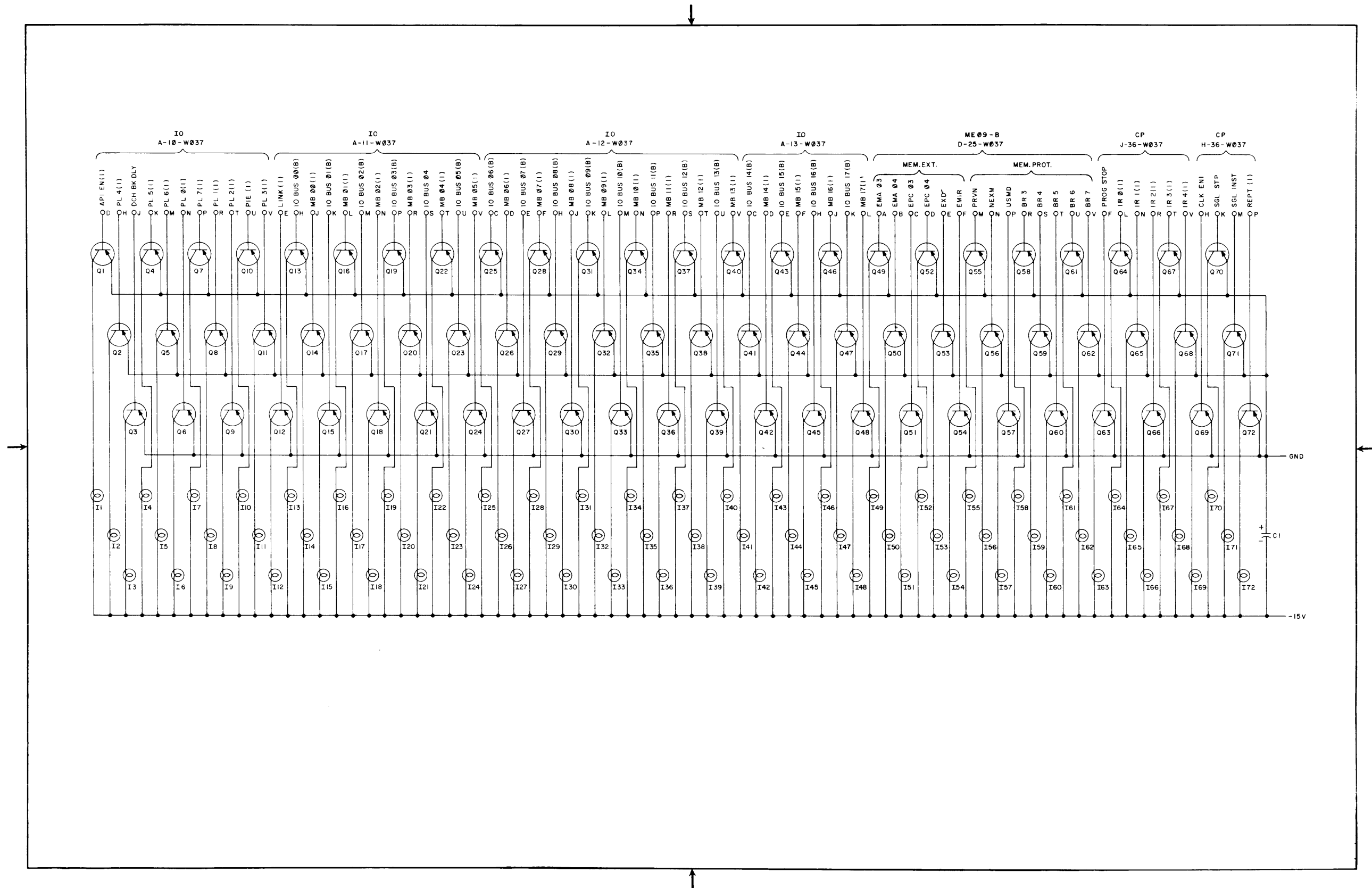


UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE 10% 1/4W 10%
CAPACITORS ARE 0.1MFD DISK, SPRAGUE
WIRE IS #22 GAUGE (STANDARD)

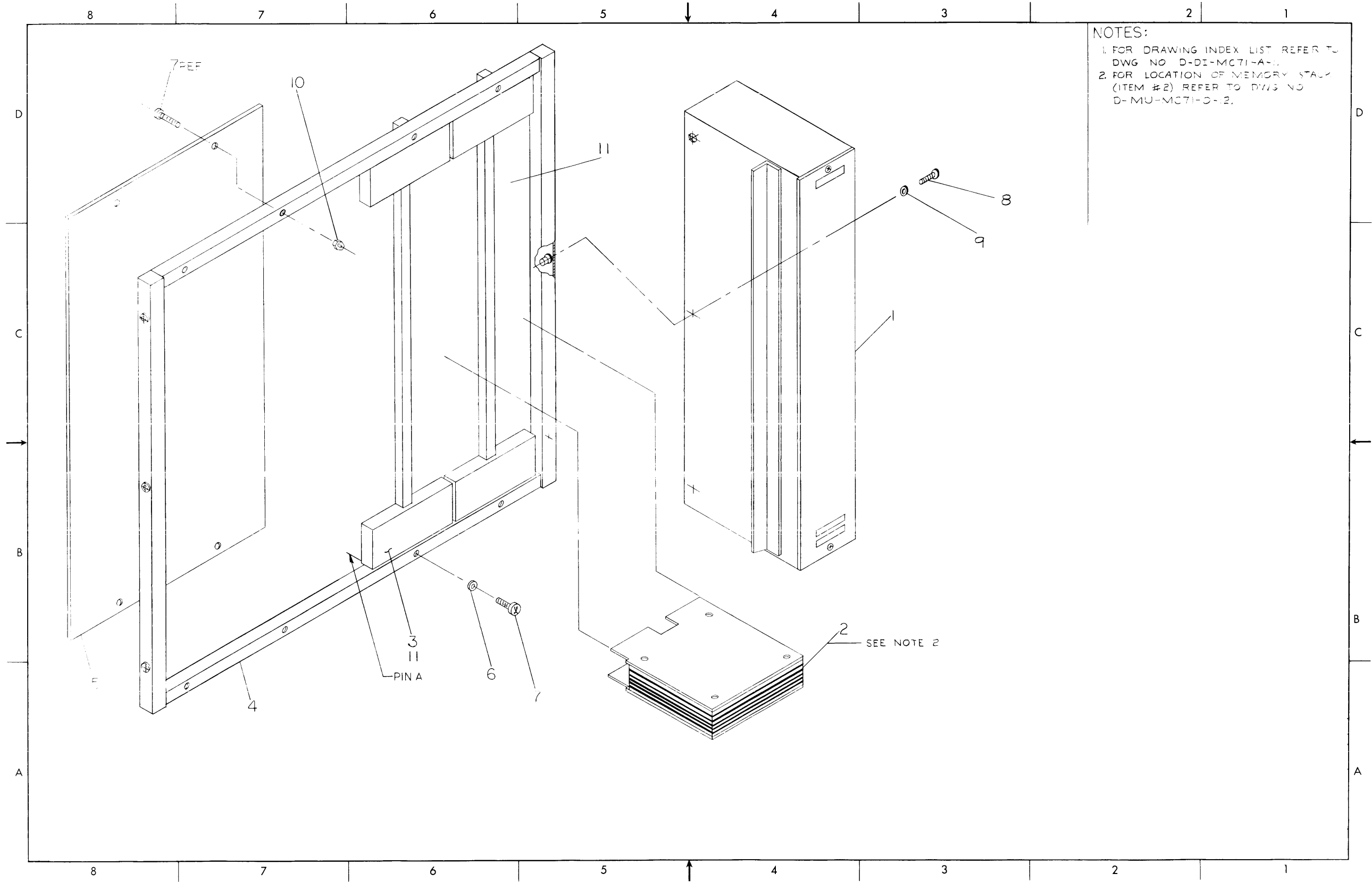
SP/6 POL-5PCS
LOCK
NORMAL
MAINTENANCE
EXAMINE
DEPOSIT



D-CS-5408018-0-1 PDP-9/L Console Switch Board

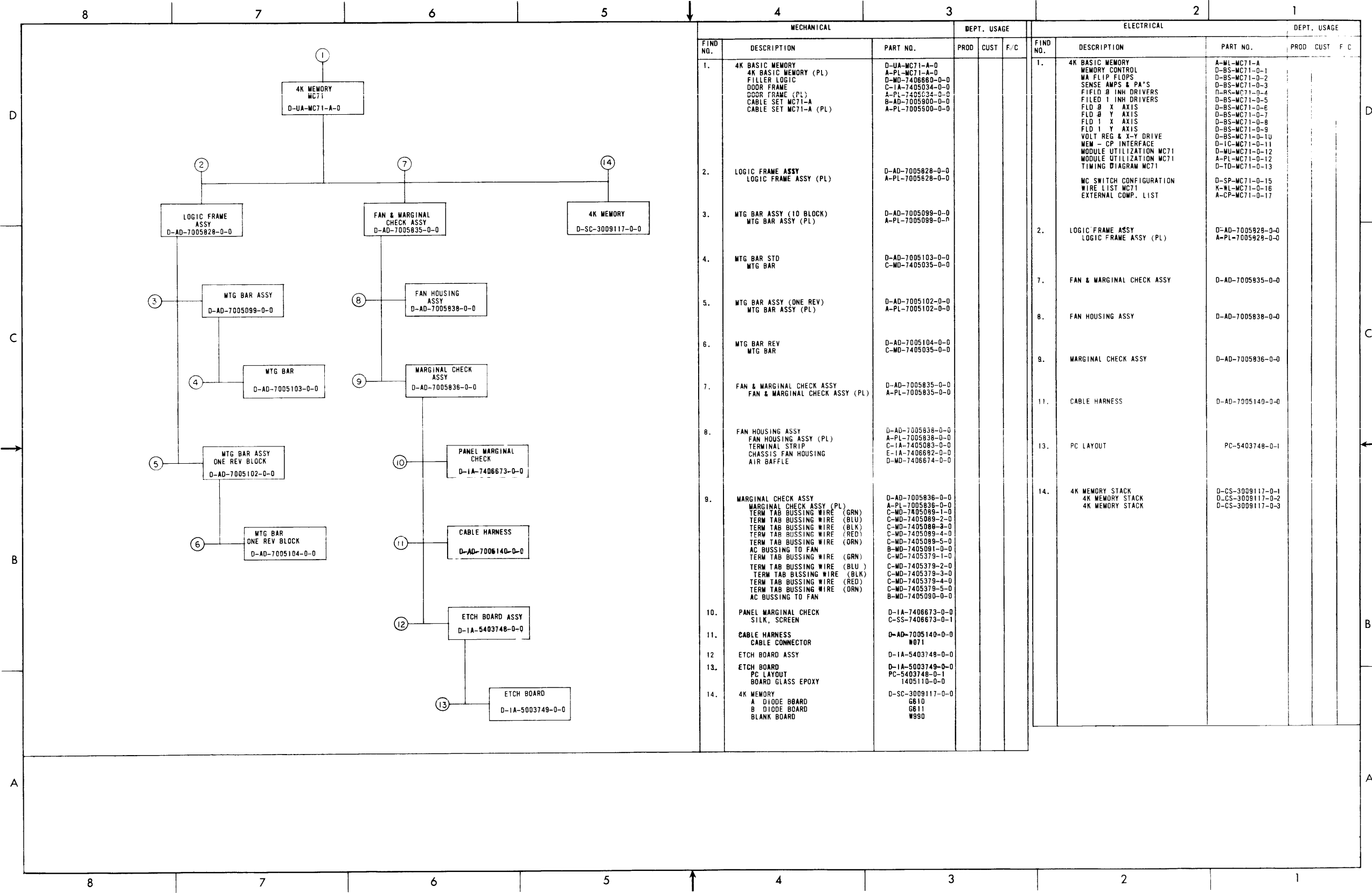


D-CS-5408020-0-1 PDP-9/L Console Light Board

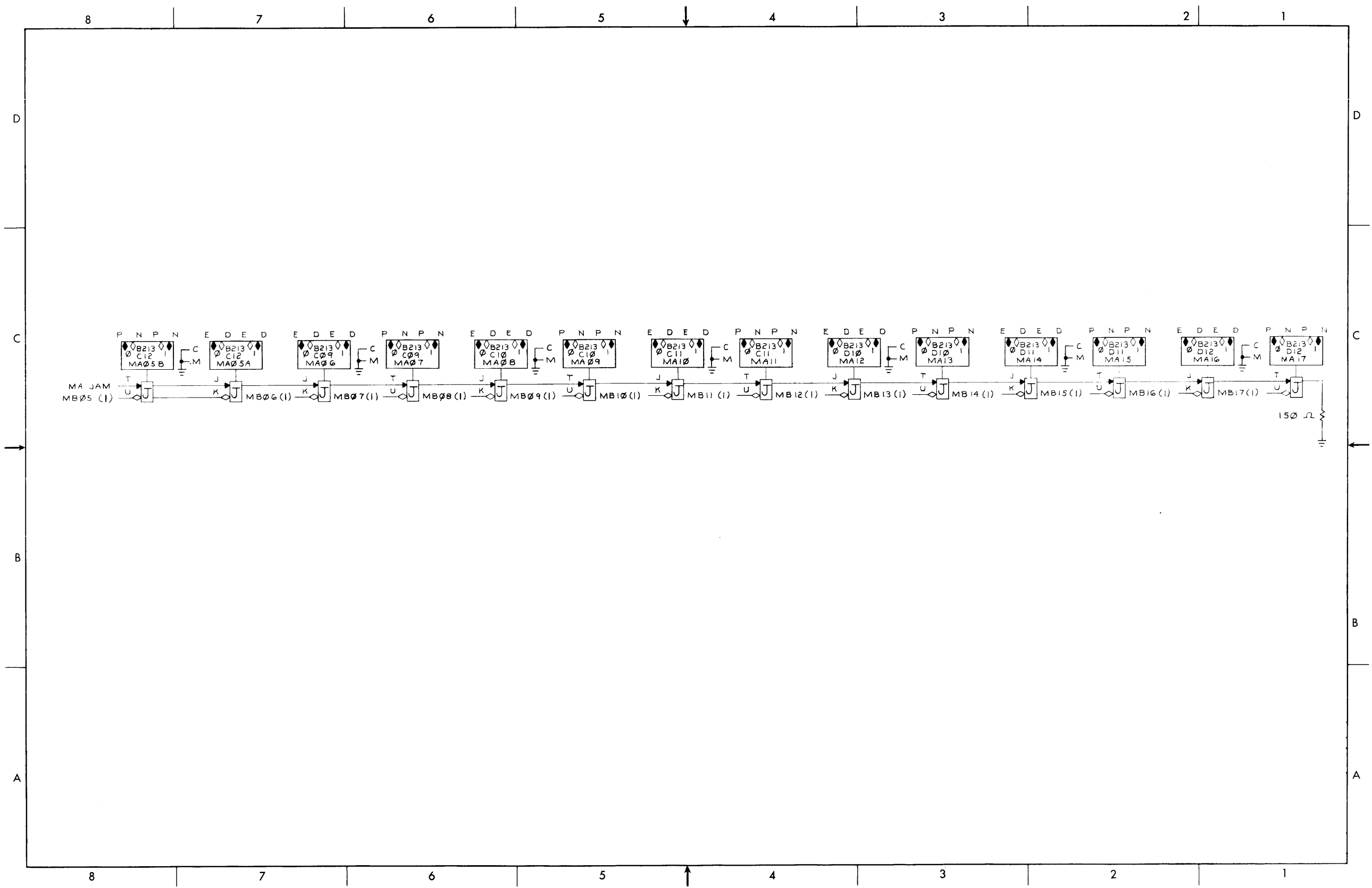


NOTES:
 1. FOR DRAWING INDEX LIST REFER TO DWG NO D-DI-MC71-A-1.
 2. FOR LOCATION OF MEMORY STACK (ITEM #2) REFER TO DWG NO D-MU-MC71-C-2.

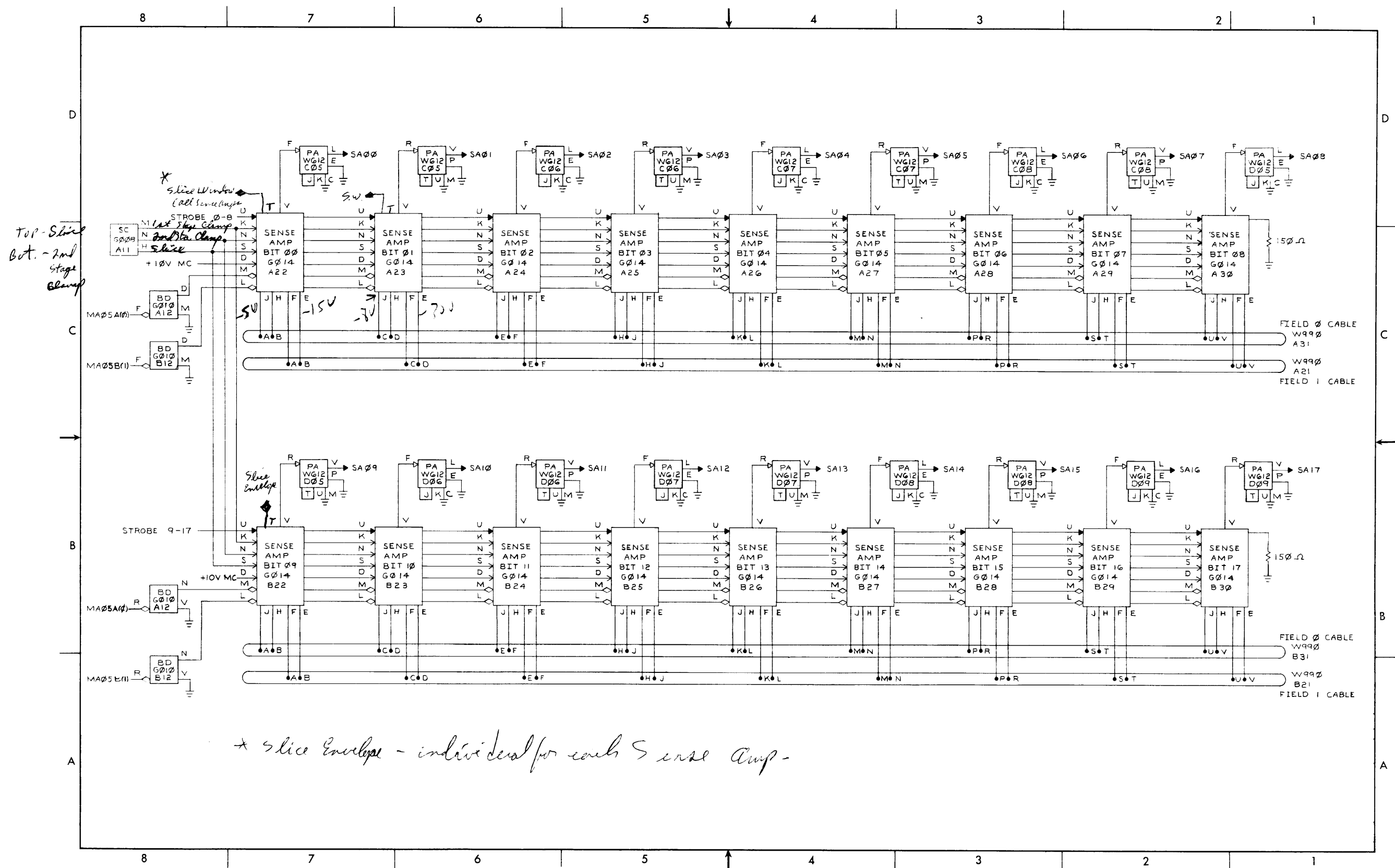
D-UA-MC71-A-0 4K Basic Memory



D-DI-MC71-A-1 Drawing Index List MC71-A



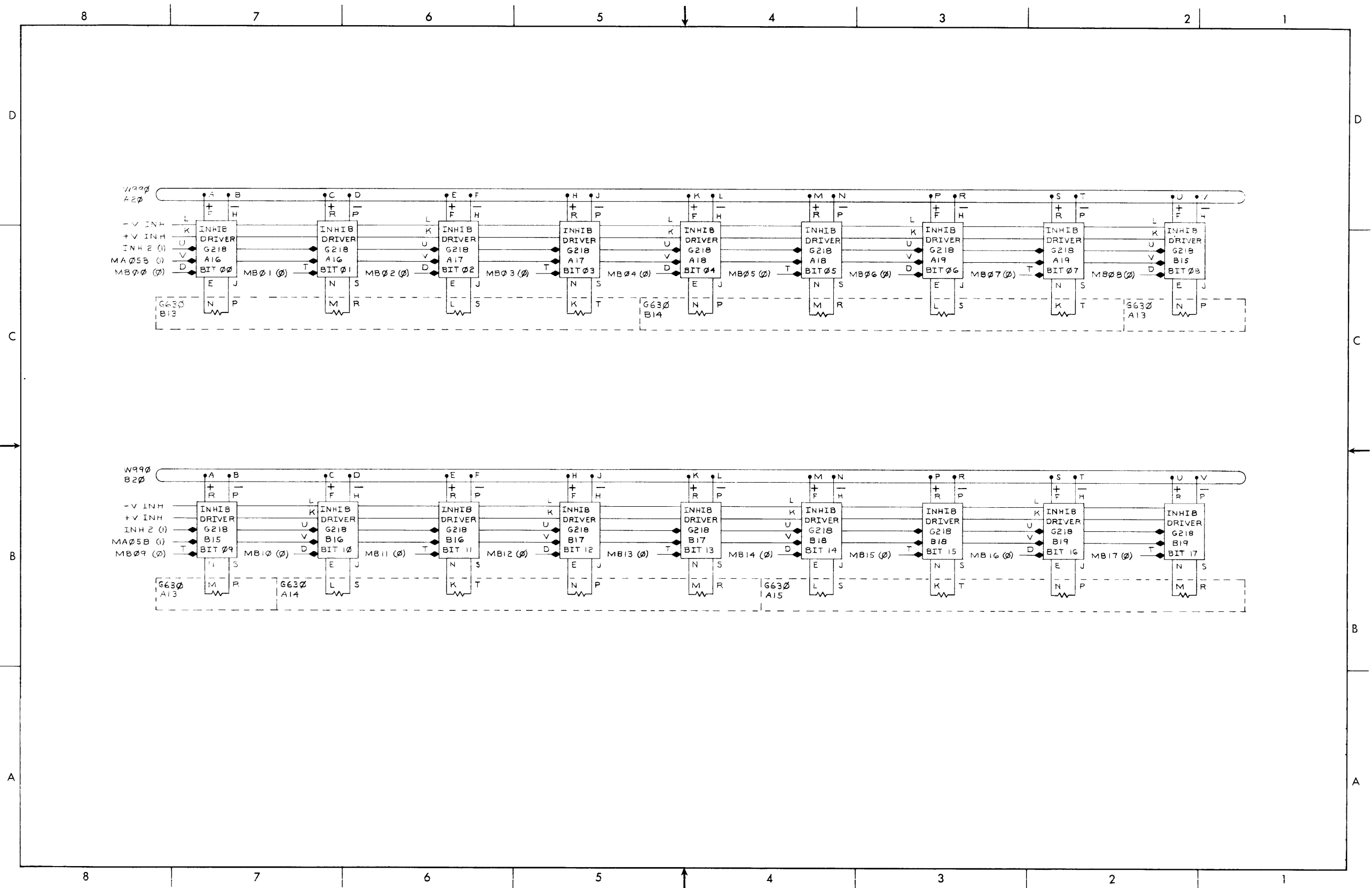
D-BS-MC71-0-2 MA Flip-Flops



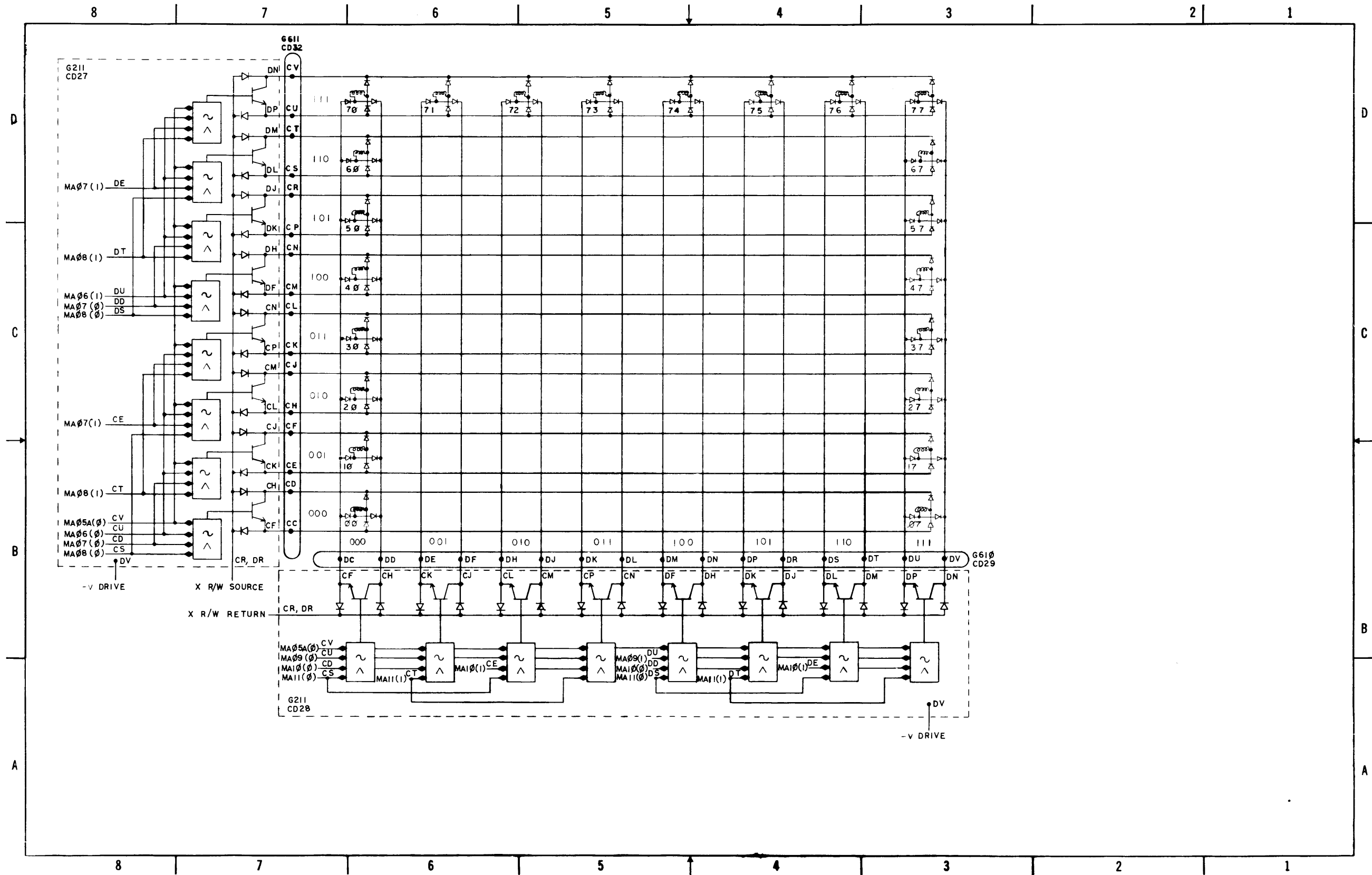
D-BS-MC71-0-3 Sense Amps and PA's



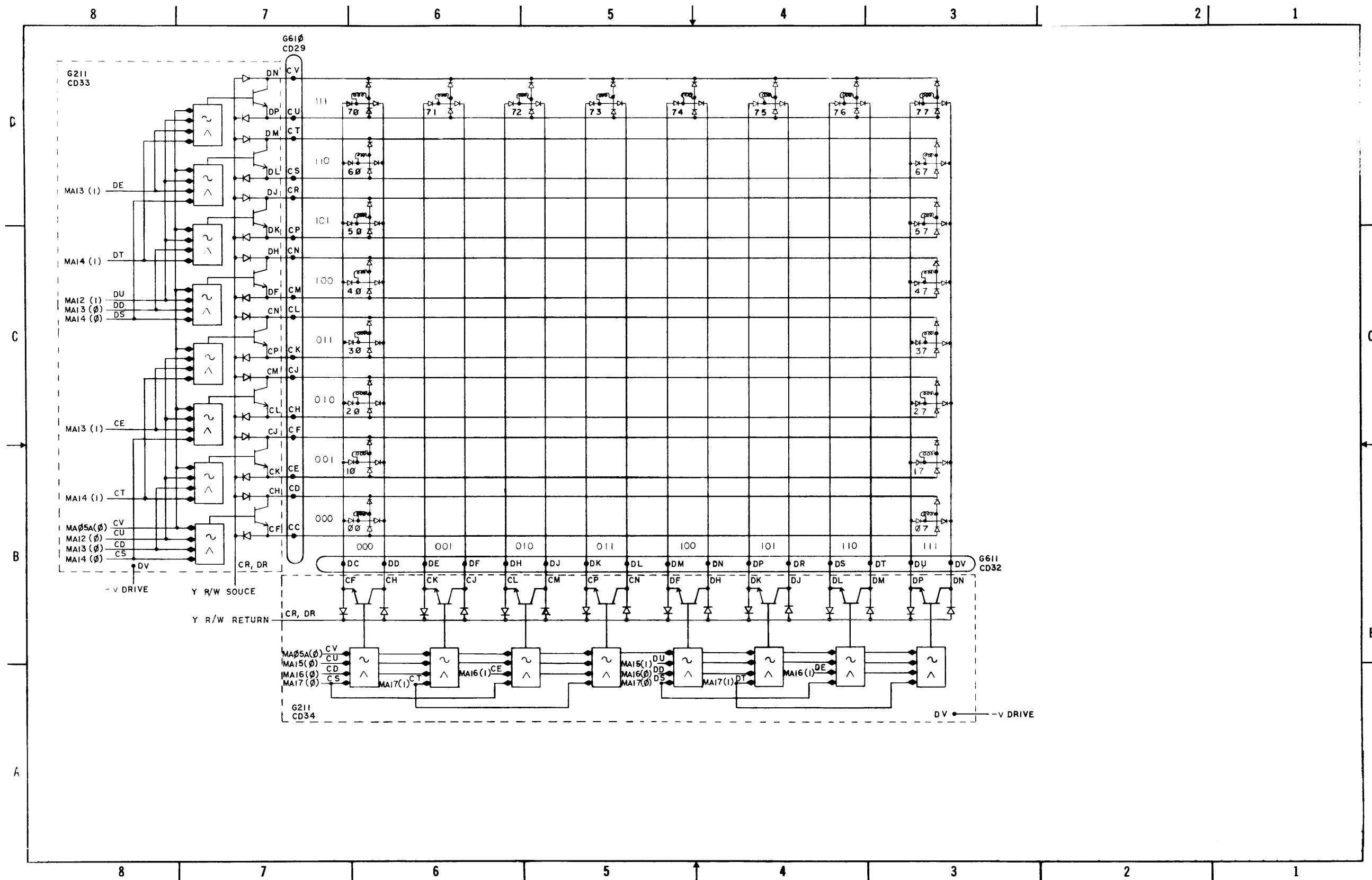
D-BS-MC71-0-4 Inhibit Drivers Field 0



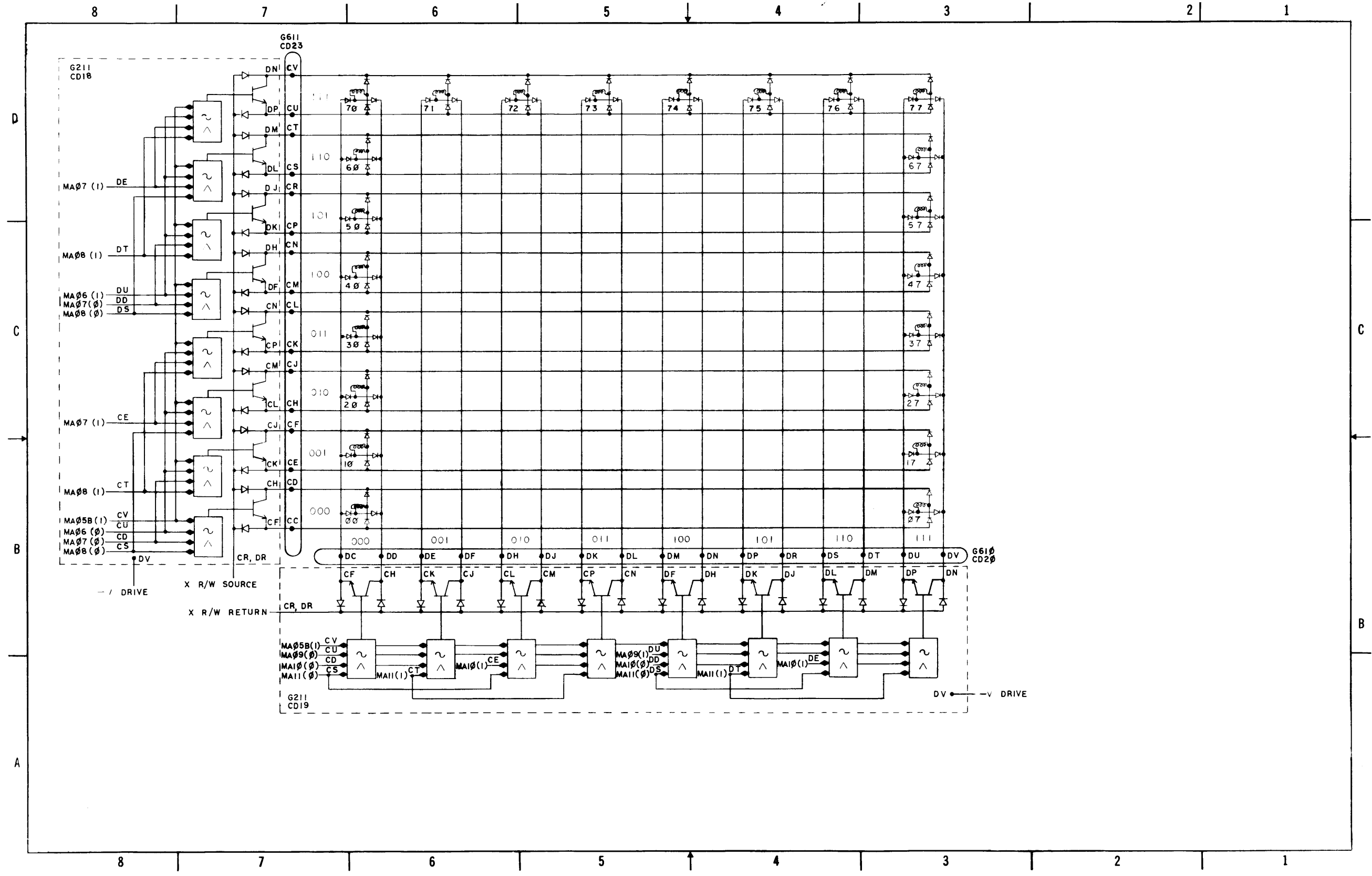
D-BS-MC71-0-5 Inhibit Drivers Field 1



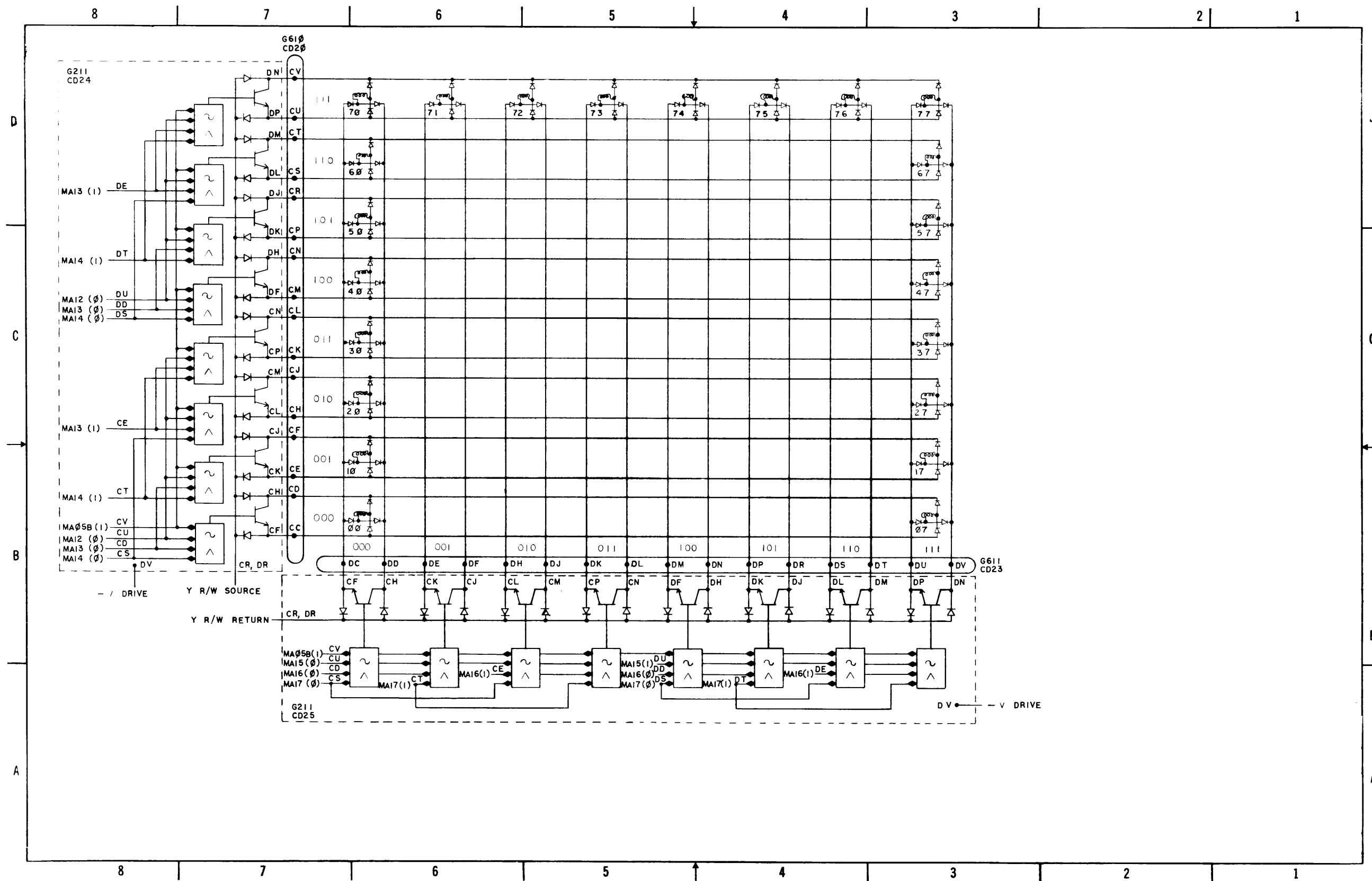
D-BS-MC71-0-6 X Axis Field 0



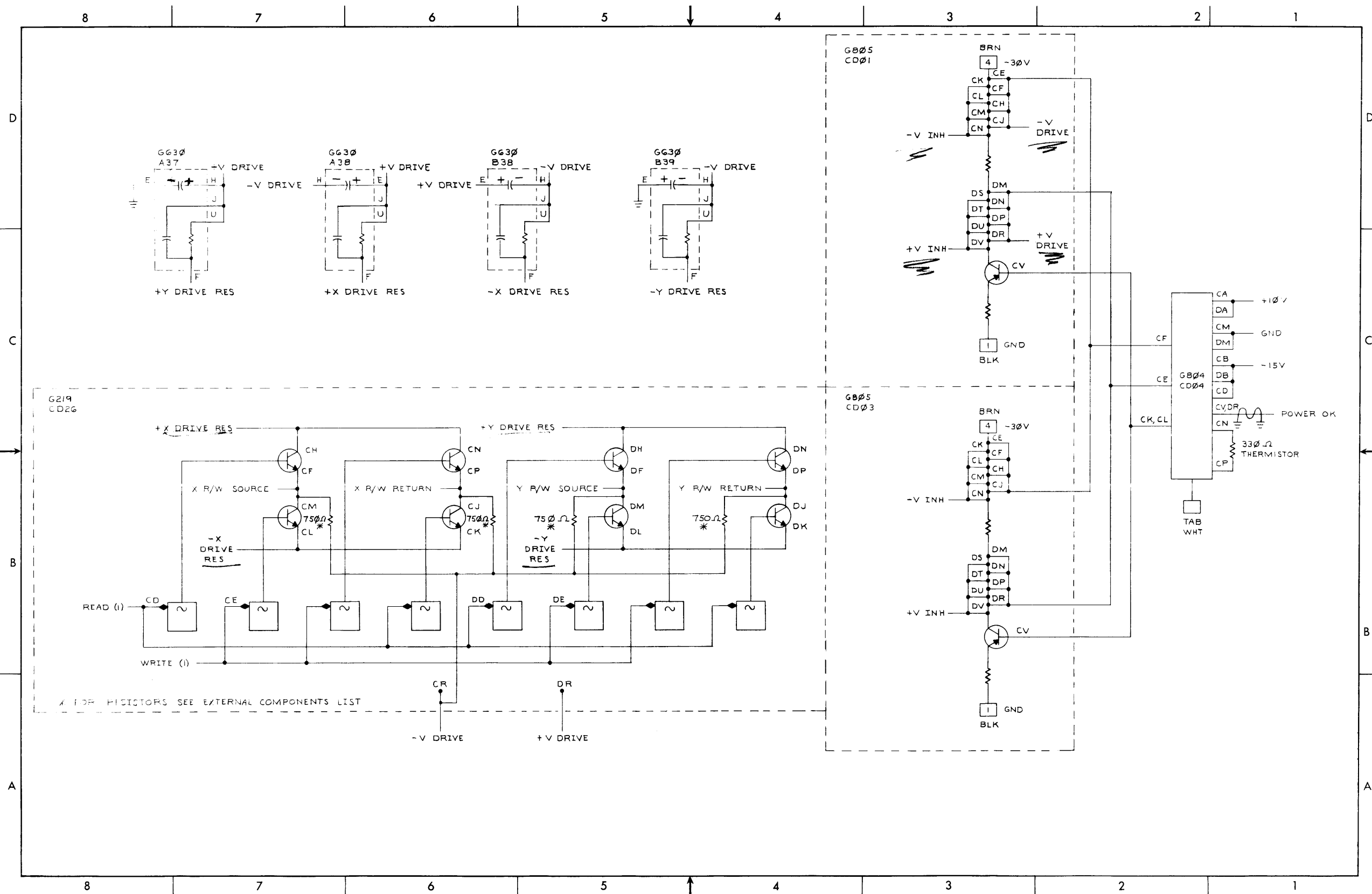
D-BS-MC71-0-7 Y Axis Field 0



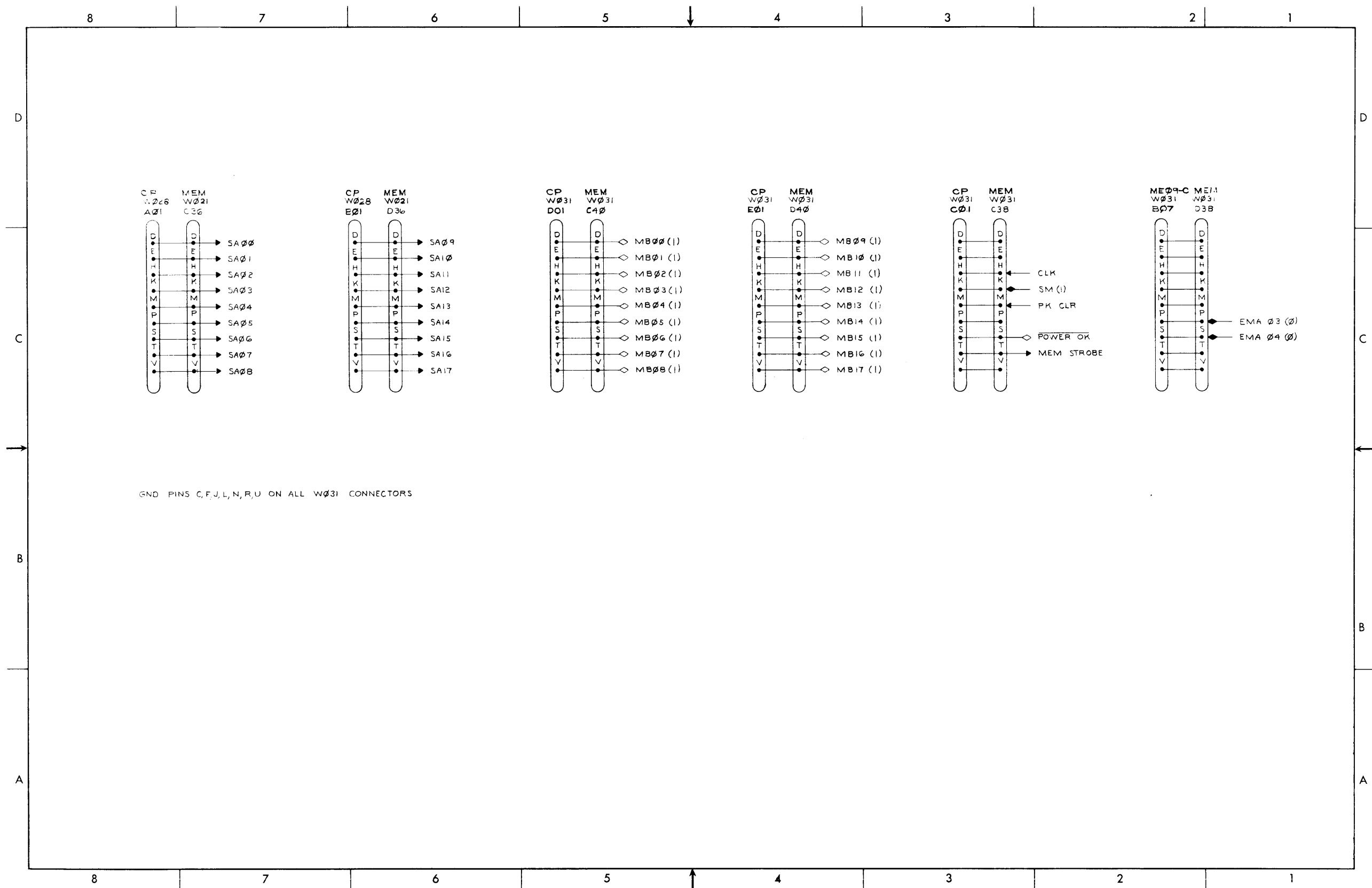
D-BS-MC71-0-8 X Axis Field 1



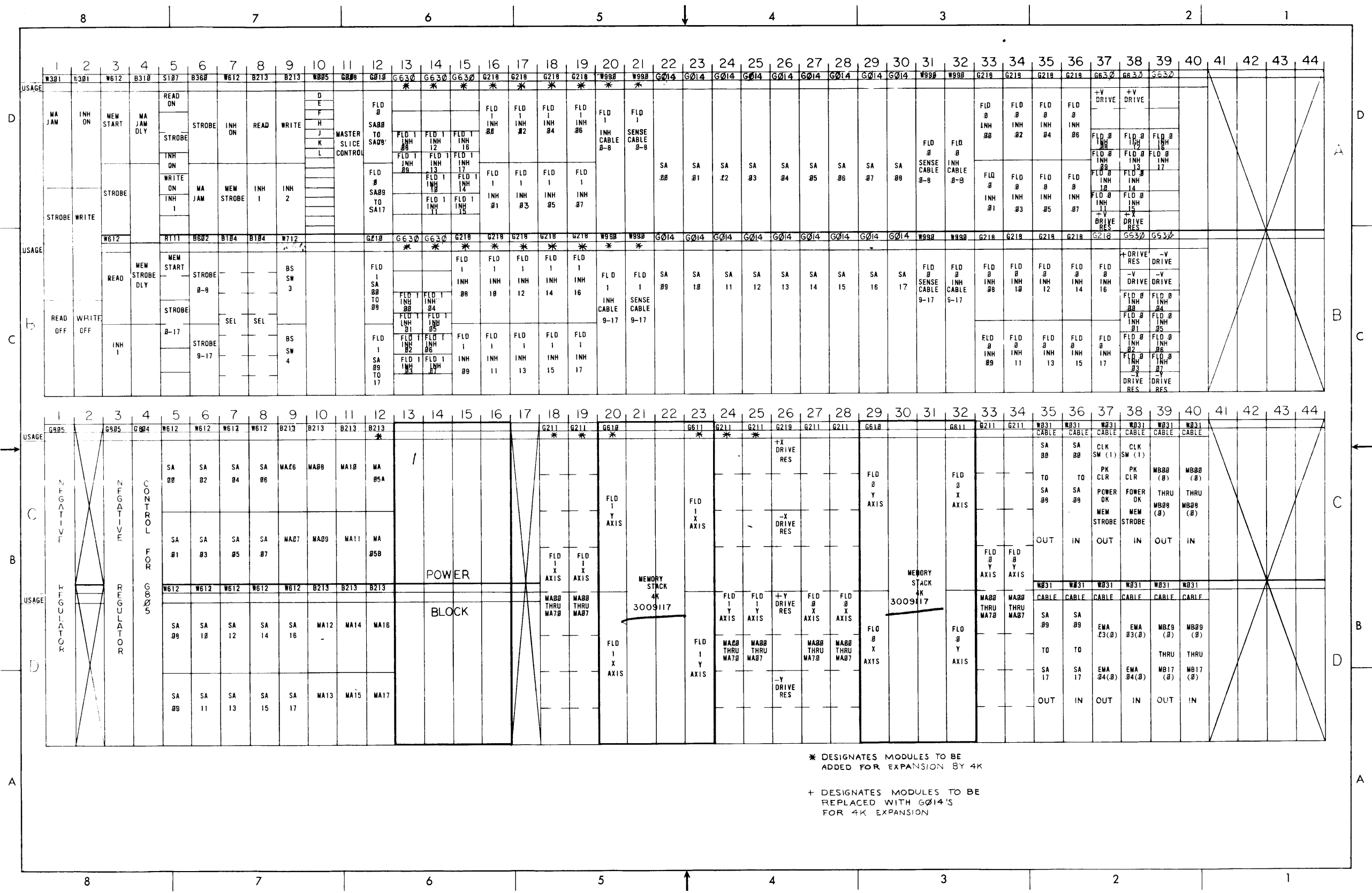
D-BS-MC71-0-9 Y Axis Field 1



D-BS-MC71-0-10 Voltage Regulator and X-Y Drive



D-IC-MC71-0-11 Memory - CP Interface



* DESIGNATES MODULES TO BE ADDED FOR EXPANSION BY 4K
 + DESIGNATES MODULES TO BE REPLACED WITH G014'S FOR 4K EXPANSION

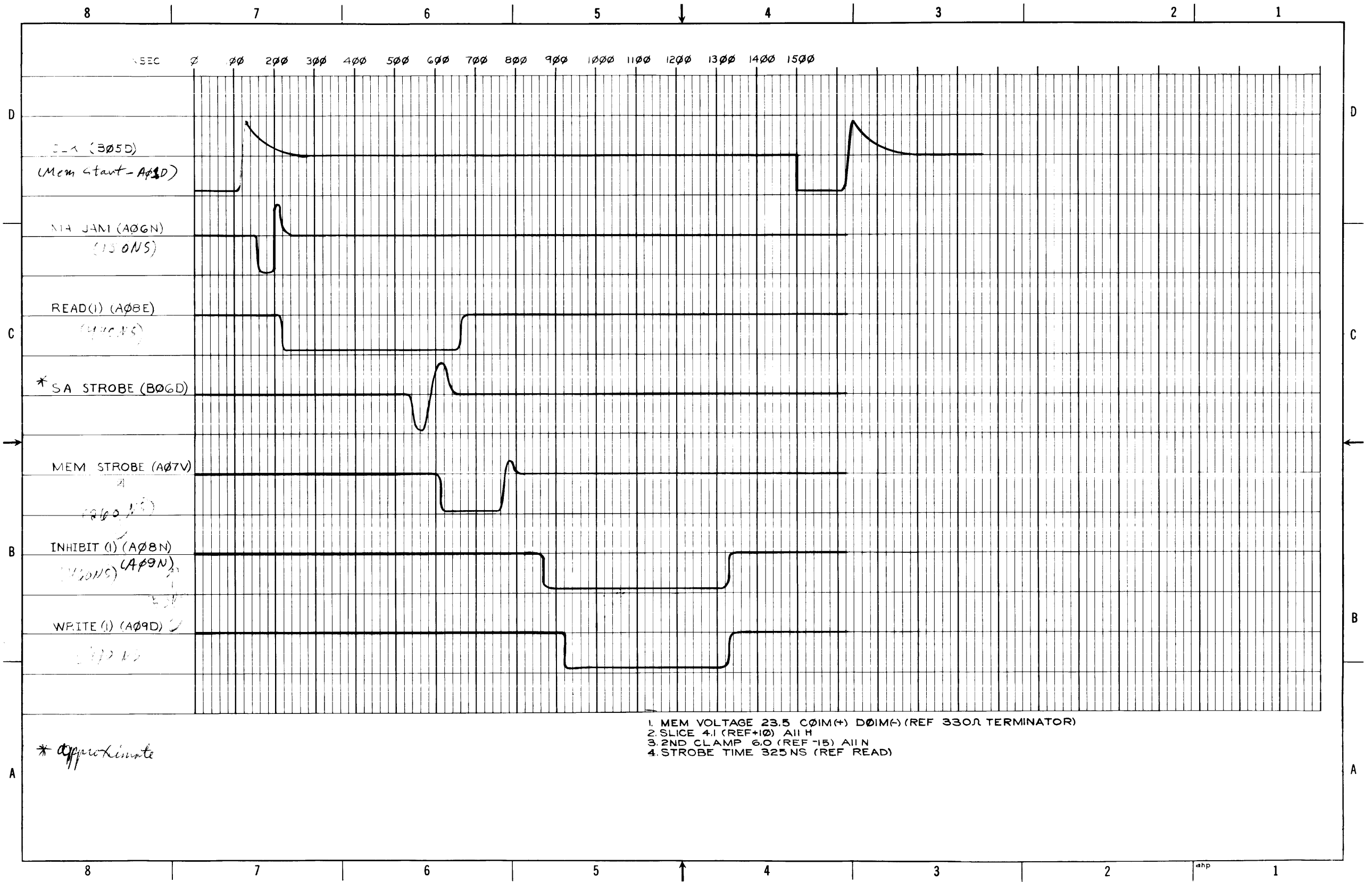
D-MU-MC71-0-12 Module Utilization

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			QUANTITY													
PARTS LIST			MC71A	MC71B												
ITEM NO.	DWG. NO.	DESCRIPTION														
	B104	INVERTER	2	0												
	B213	JAM FLIP-FLOP	8	1												
	B360	DELAY WITH PULSE AMPLIFIER	1	0												
	B310	DELAY	1	0												
	B602	PULSE AMPLIFIER	1	0												
	W712	<i>Bank Select Sense</i>	1	0												
	G008	MASTER SLICE CONTROL	1	0												
	G010	SENSE AMP SELECTOR	2	0												
	G014		18	0												
	G211	CURRENT DRIVER	4	4												
	G218	INHIBIT DRIVER	9	9												
	G219	MEMORY SELECTOR	1	0												

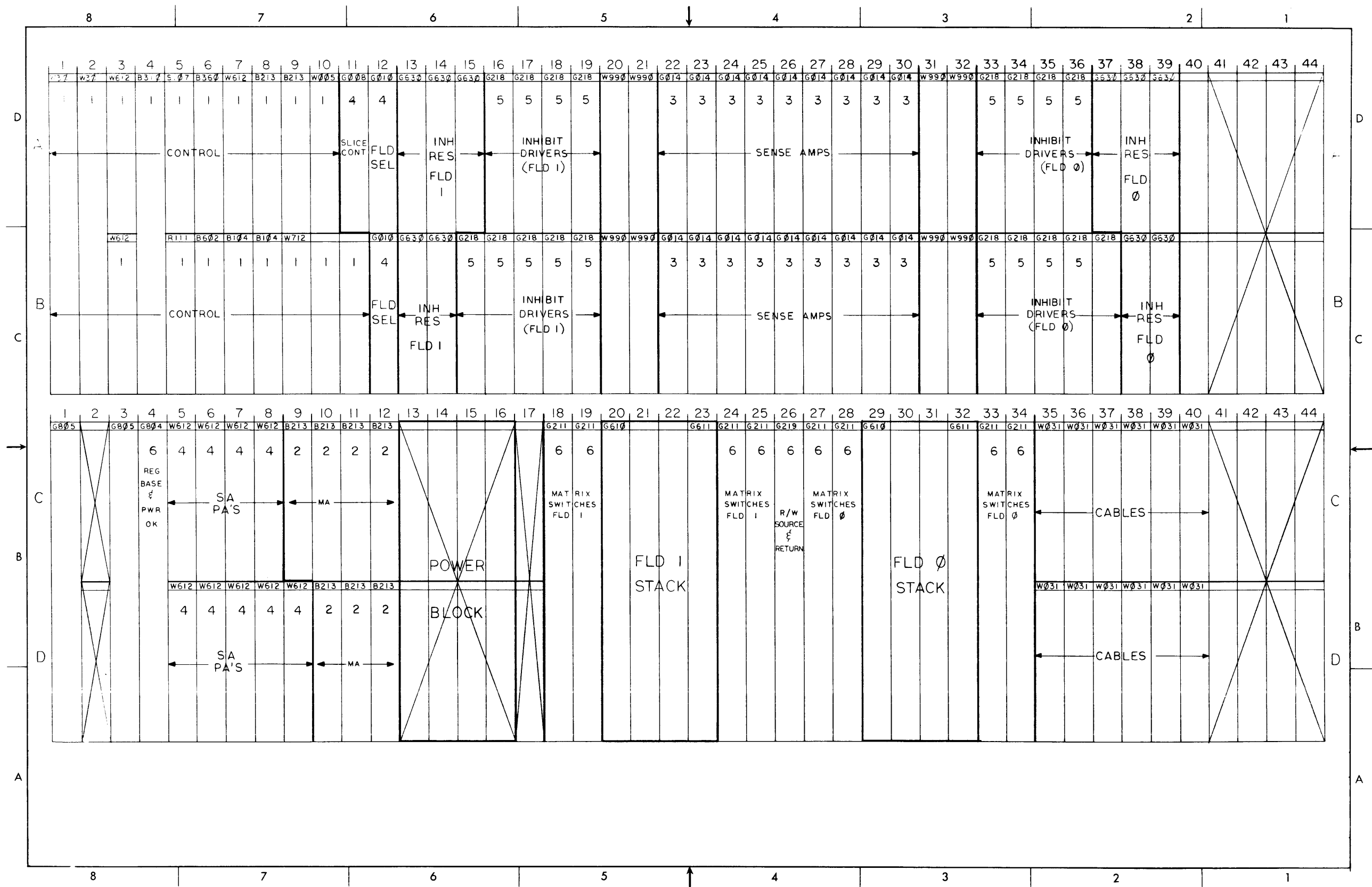
A-PL-MC71-0-12 Module Utilization List (Sheet 1)

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS			QUANTITY													
PARTS LIST			MC71A	MC71B												
ITEM NO.	DWG. NO.	DESCRIPTION														
	G030	RESISTOR BOARD	5	5												
	G004	CONTROL FOR G005	1	0												
	G005	NEGATIVE REGULATOR	2	0												
	R111	EXPANDABLE NAND/NOR GATE	1	0												
	S107	INVERTER	1	0												
	W005	CLAMPED LOAD	1	0												
	W301	DELAY LINE	2	0												
	W612	<i>Pulse Comp</i>	12	0												
	D-SC-3009117-0-0	MEMORY STACK 4K	1	1												

A-PL-MC71-0-12 Module Utilization List (Sheet 2)







D-TD-MC71-0-13 Timing Diagram

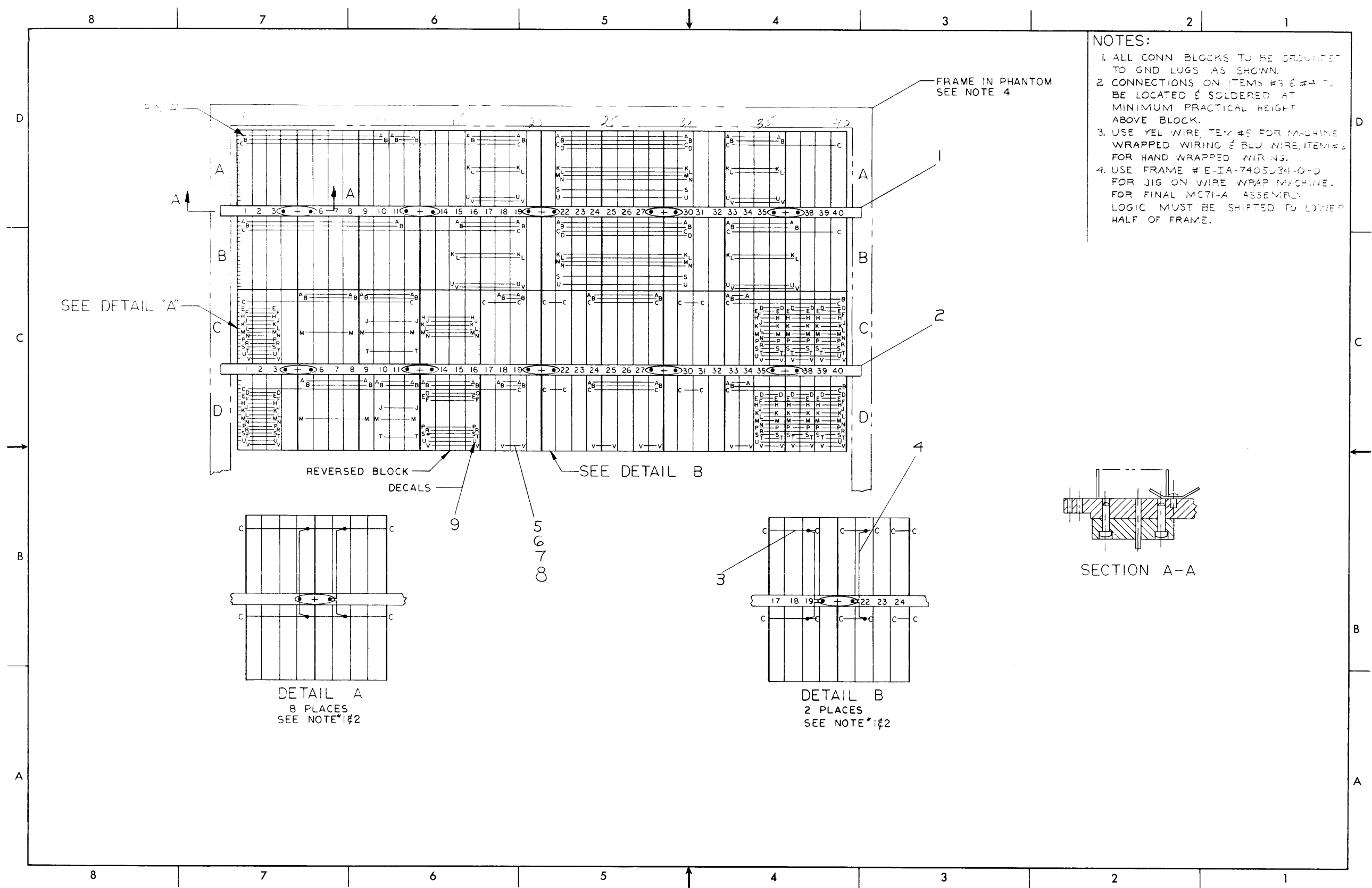


D-SP-MC71-0-15 MC Switch Configuration

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COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
STACK CLAMP	750 OHM 1W 5%		C26F	C22F	
STACK CLAMP	750 OHM 1W 5%		C26J	C22J	
STACK CLAMP	750 OHM 1W 5%		D26F	D22F	
STACK CLAMP	750 OHM 1W 5%		D26J	D22J	
CLK	150 OHM 1/4W 5%		B05D	C05C	
STROBE	150 OHM 1/4W 5%		A30U	B30C	
STROBE	150 OHM 1/4W 5%		B30U	B30C	
MA JAM	150 OHM 1/4W 5%		D12T	D12M	
MEM STROBE	1K Ω 1/4W 5%		C38T	C38C	
* MA05A(0) 	JUMPER		C12E	A10U	
* MA05A(0) 	JUMPER		C12D	C12C	
* MA05B(0) 	JUMPER		C12P	A10V	
* MA05B(0) 	JUMPER		C12N	C12M	
* JUMPERS TO REMOVE FOR	BE ADDED BK OPERATION	FOR	4K OPERATION		

A-CP-MC71-0-17 MC71 Memory Panel



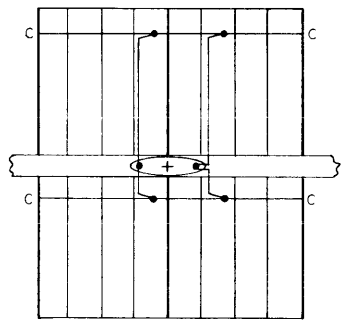
- NOTES:**
1. ALL CONN BLOCKS TO BE GROUNDED TO GND LUGS AS SHOWN.
 2. CONNECTIONS ON ITEMS #3 & #4 TO BE LOCATED & SOLDERED AT MINIMUM PRACTICAL HEIGHT ABOVE BLOCK.
 3. USE YEL WIRE, ITEM #5 FOR MACHINE WRAPPED WIRING & BLU WIRE, ITEM #3 FOR HAND WRAPPED WIRING.
 4. USE FRAME # E-IA-7405039-0-0 FOR JIG ON WIRE WRAP MACHINE. FOR FINAL MCT1-A ASSEMBLY LOGIC MUST BE SHIFTED TO LOWER HALF OF FRAME.

SEE DETAIL 'A'

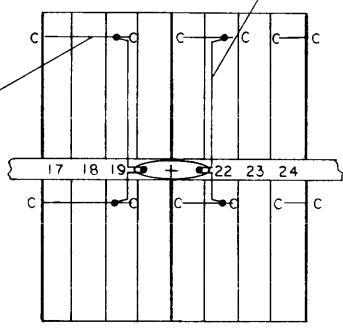
REVERSED BLOCK
DECALS

SEE DETAIL B

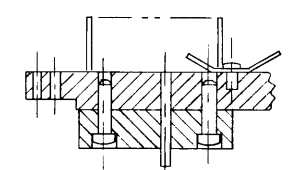
FRAME IN PHANTOM
SEE NOTE 4



DETAIL A
8 PLACES
SEE NOTE #2



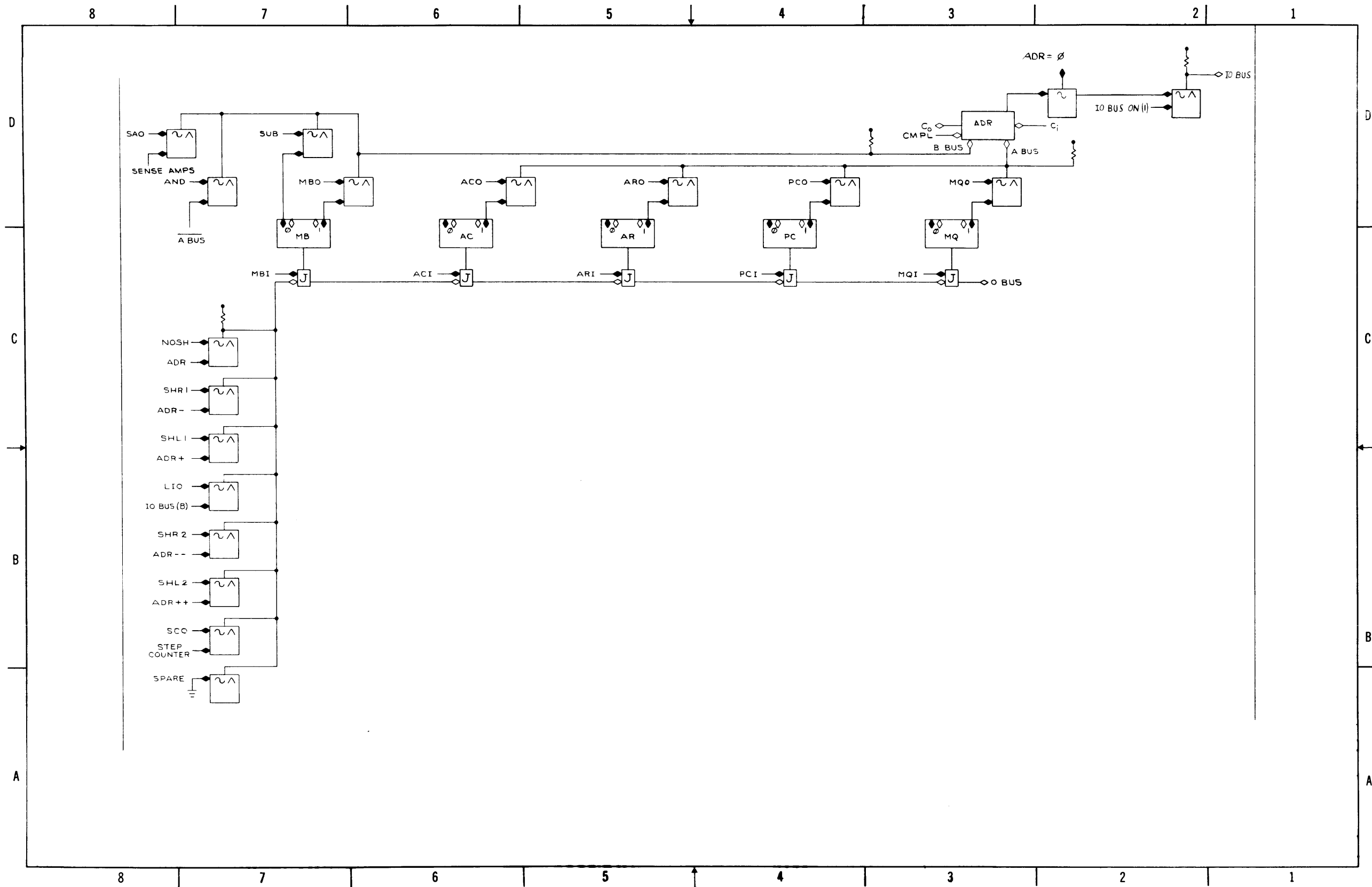
DETAIL B
2 PLACES
SEE NOTE #2



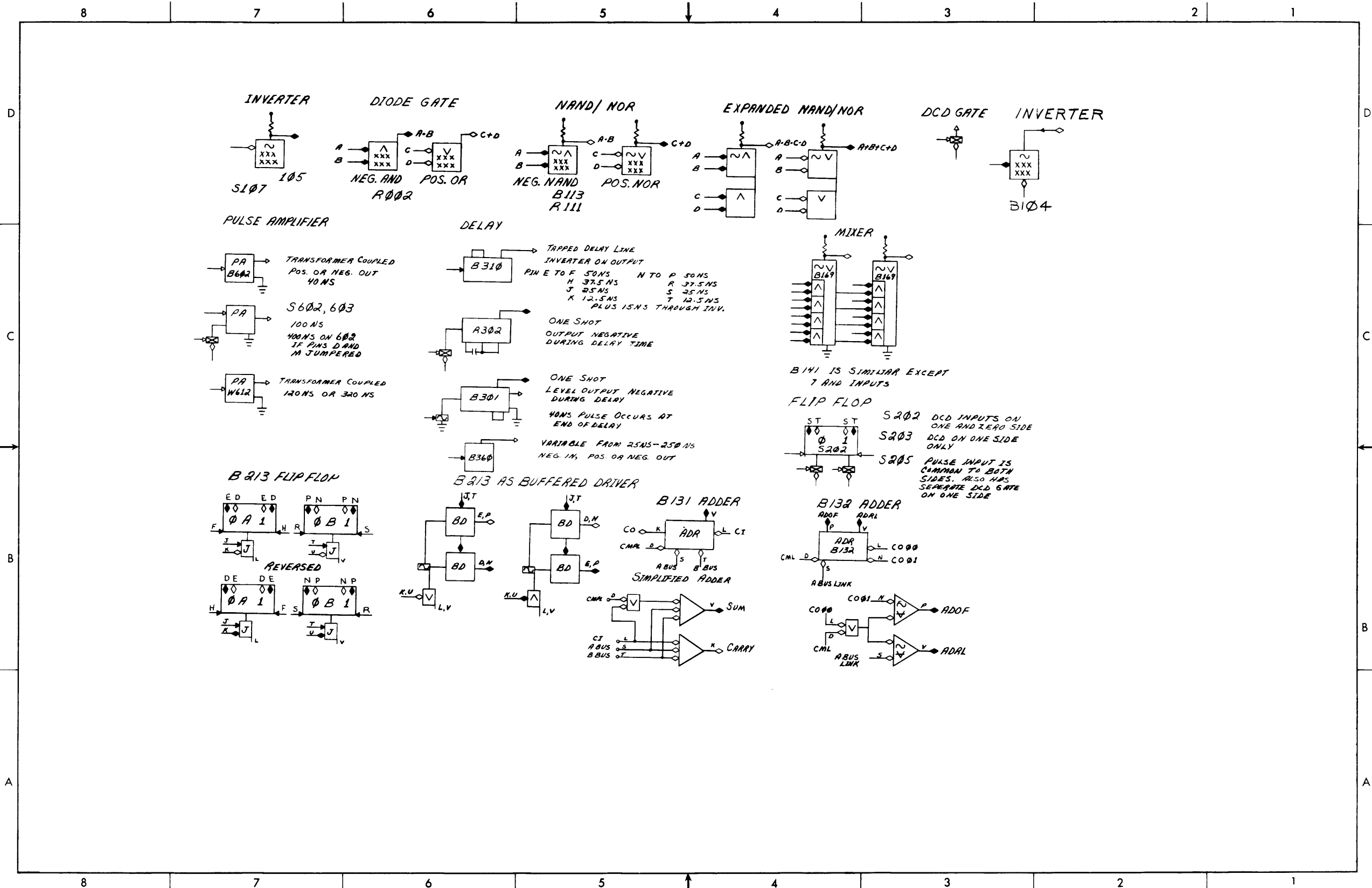
SECTION A-A

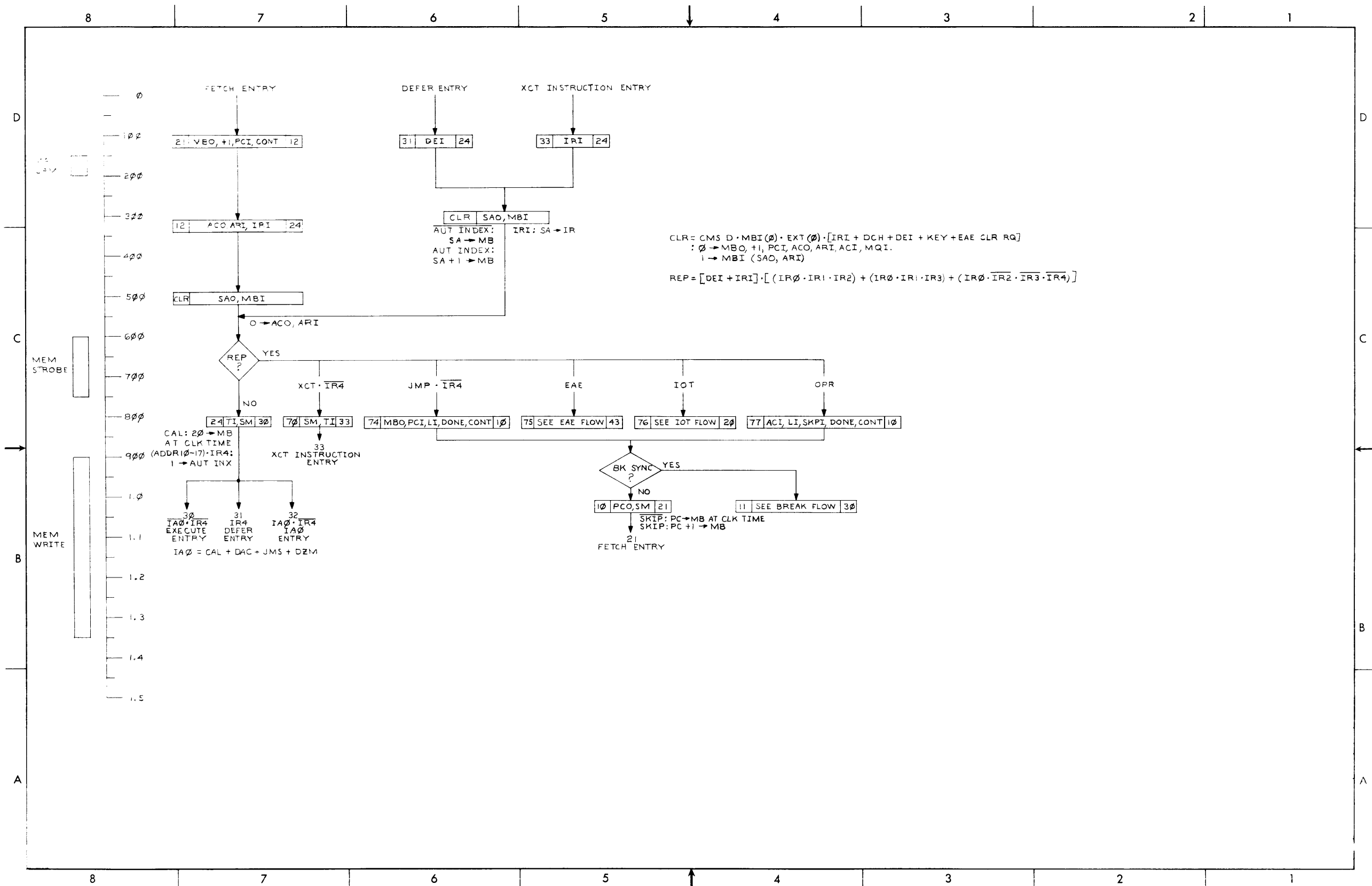
PARTS LIST		DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS		
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.
1	D-AD-7005099-0-0	1	MTG BAR ASSY (10 CONN BLOCKS)	7005099
2	D-AD-7005102-0-0	1	MTG BAR ASSY (ONE REV BLOCK)	7005102
3		A/R	VOLTAGE CHAIN	1202188
4		A/R	#24 AWG SOLID KYNAR WHT	9107470-1
5		A/R	#24 AWG SOLID KYNAR YEL	9107470-5
6		A/R	#24 AWG SOLID KYNAR BLU	9107470-10
7	K-WL-MC71-0-16	REF	WIRE LIST MC71	
8	A-CP-MC71-0-17	REF	EXTERNAL COMPONENT LIST MC71	
9	A-DC-740-11-0-0	REF	DECALS, REVERSE BLOCK	7406747

A-PL-7005828-0-0 Logic Frame Assembly

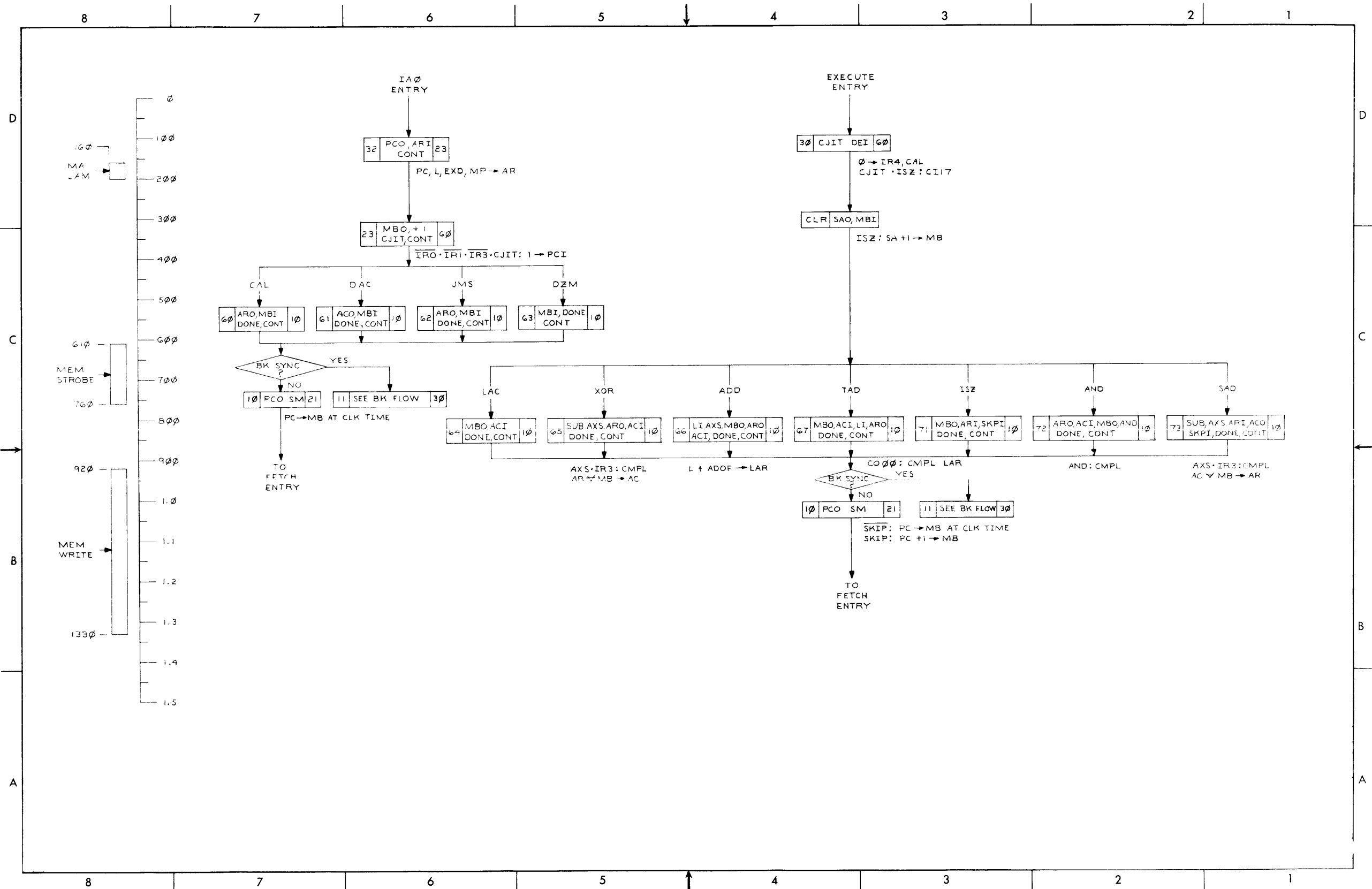


D-BS-KC09-C-1 Register Configuration

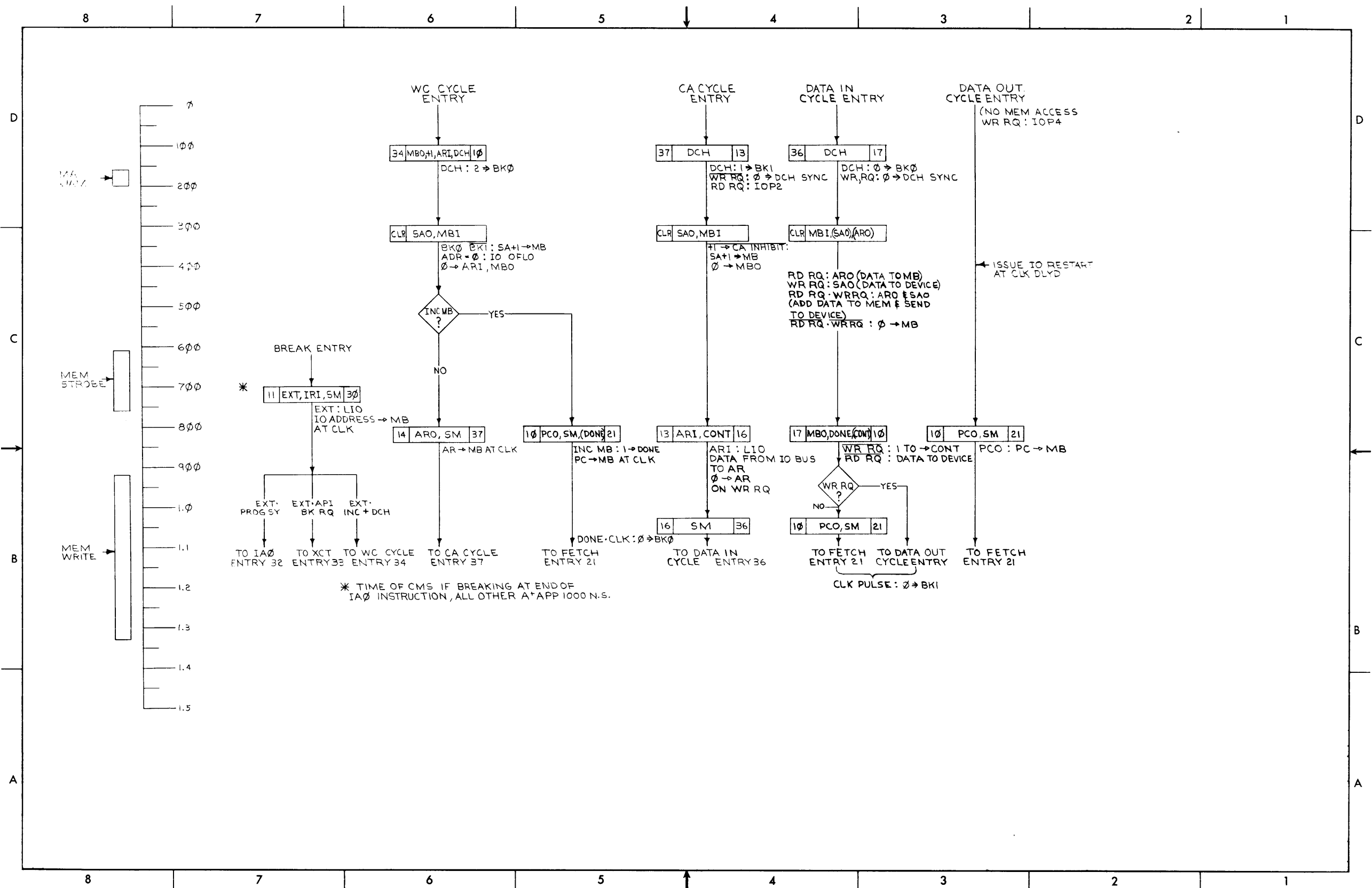




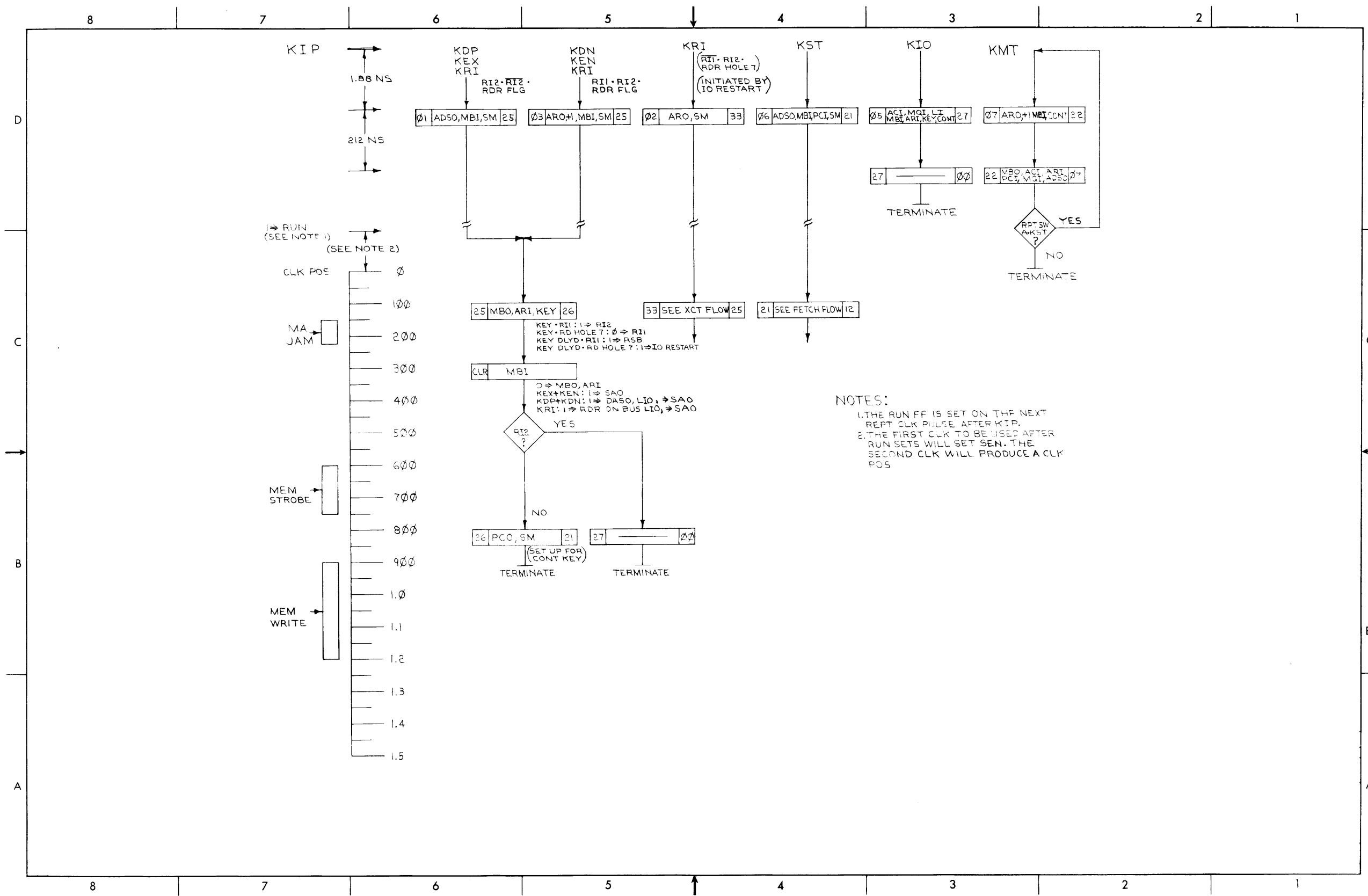
D-TD-KC09-C-3 Fetch Flow



D-TD-KC09-C-4 Execute Flow



D-TD-KC09-C-5 Break Flow

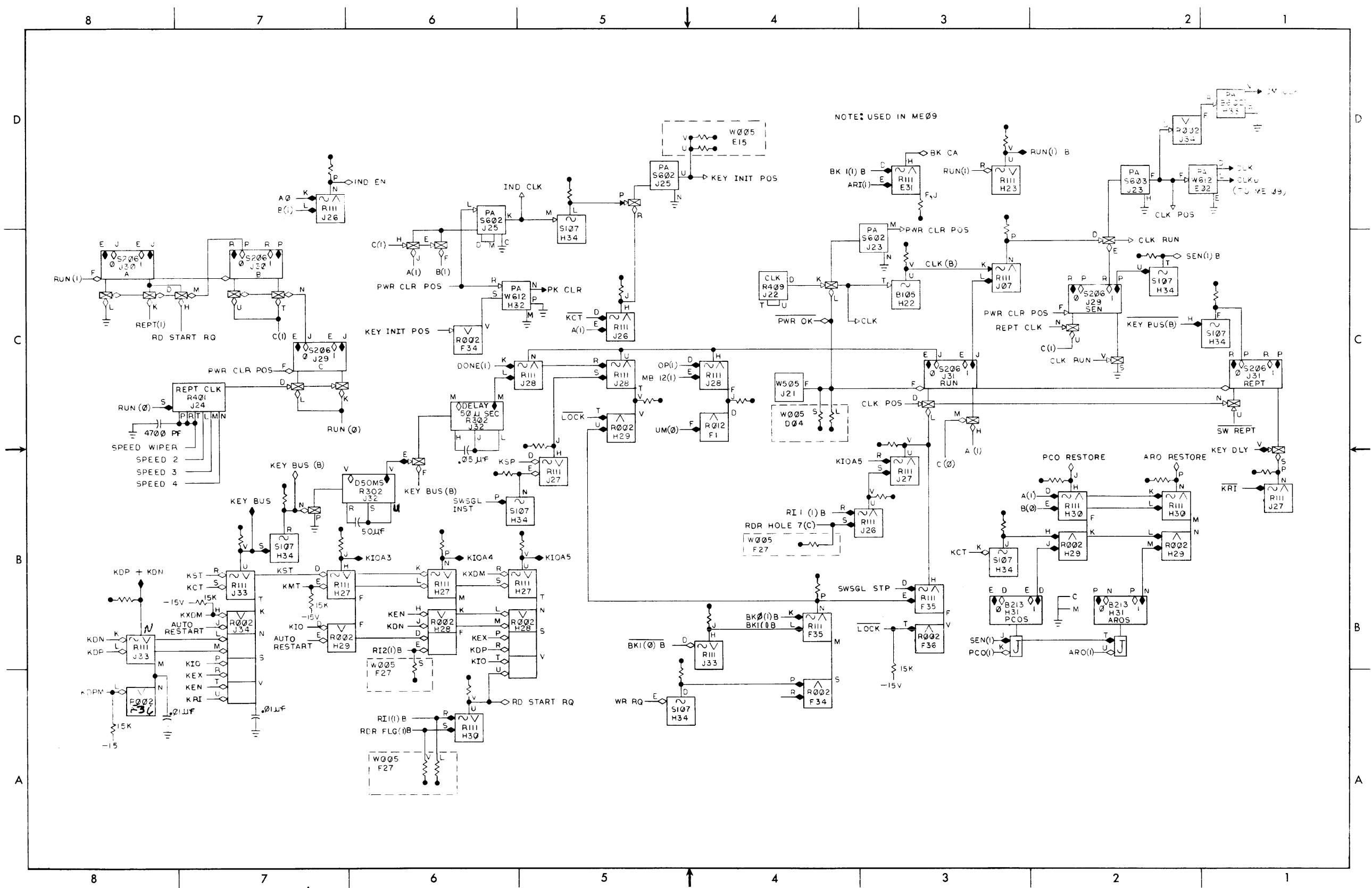


NOTES:
 1. THE RUN FF IS SET ON THE NEXT REPT CLK PULSE AFTER KIP.
 2. THE FIRST CLK TO BE USED AFTER RUN SETS WILL SET SEN. THE SECOND CLK WILL PRODUCE A CLK POS

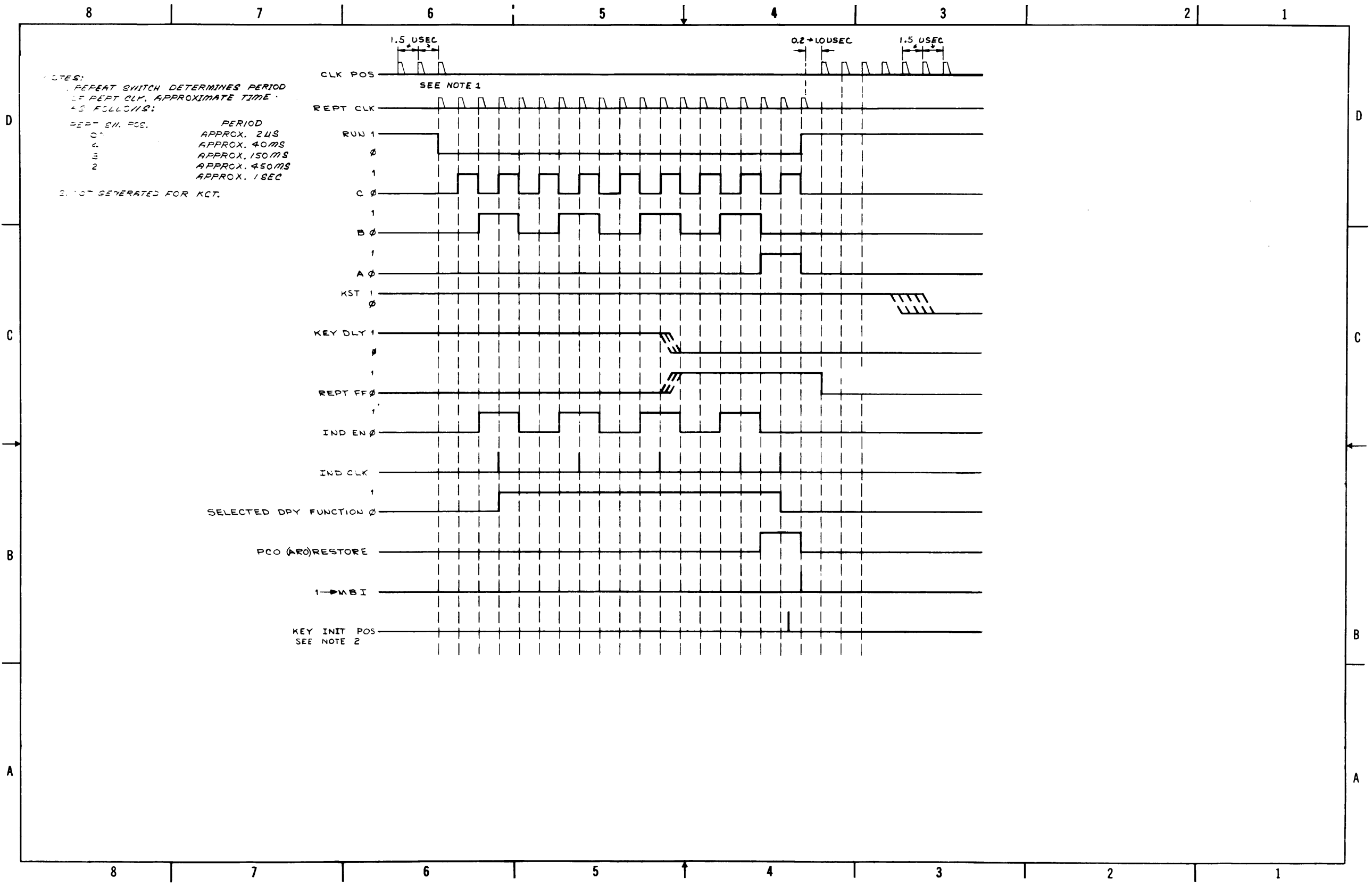
D-TD-KC09-C-6 Key Flow



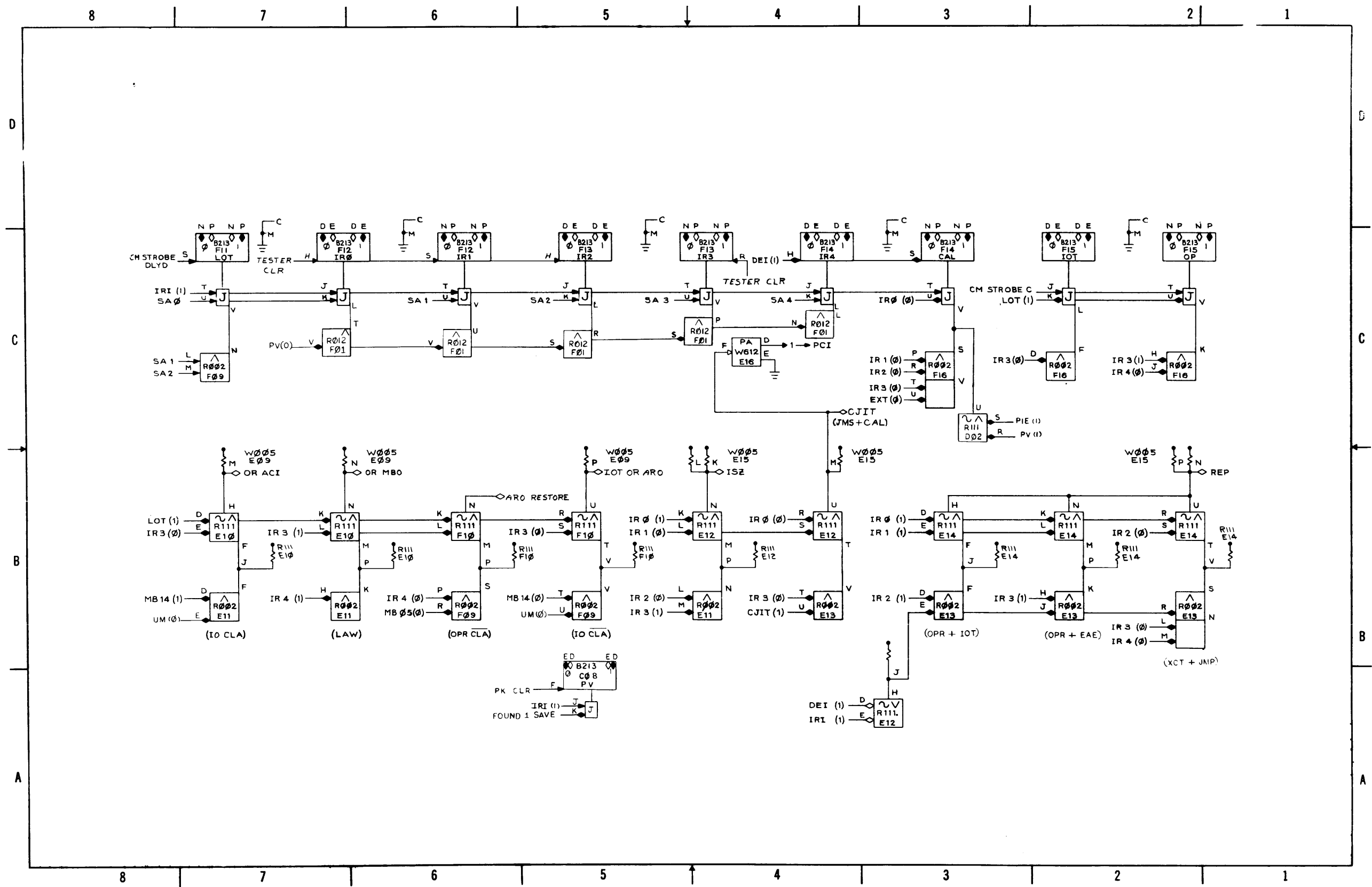
D-SP-KC09-C-9 CP MC Switch Configuration



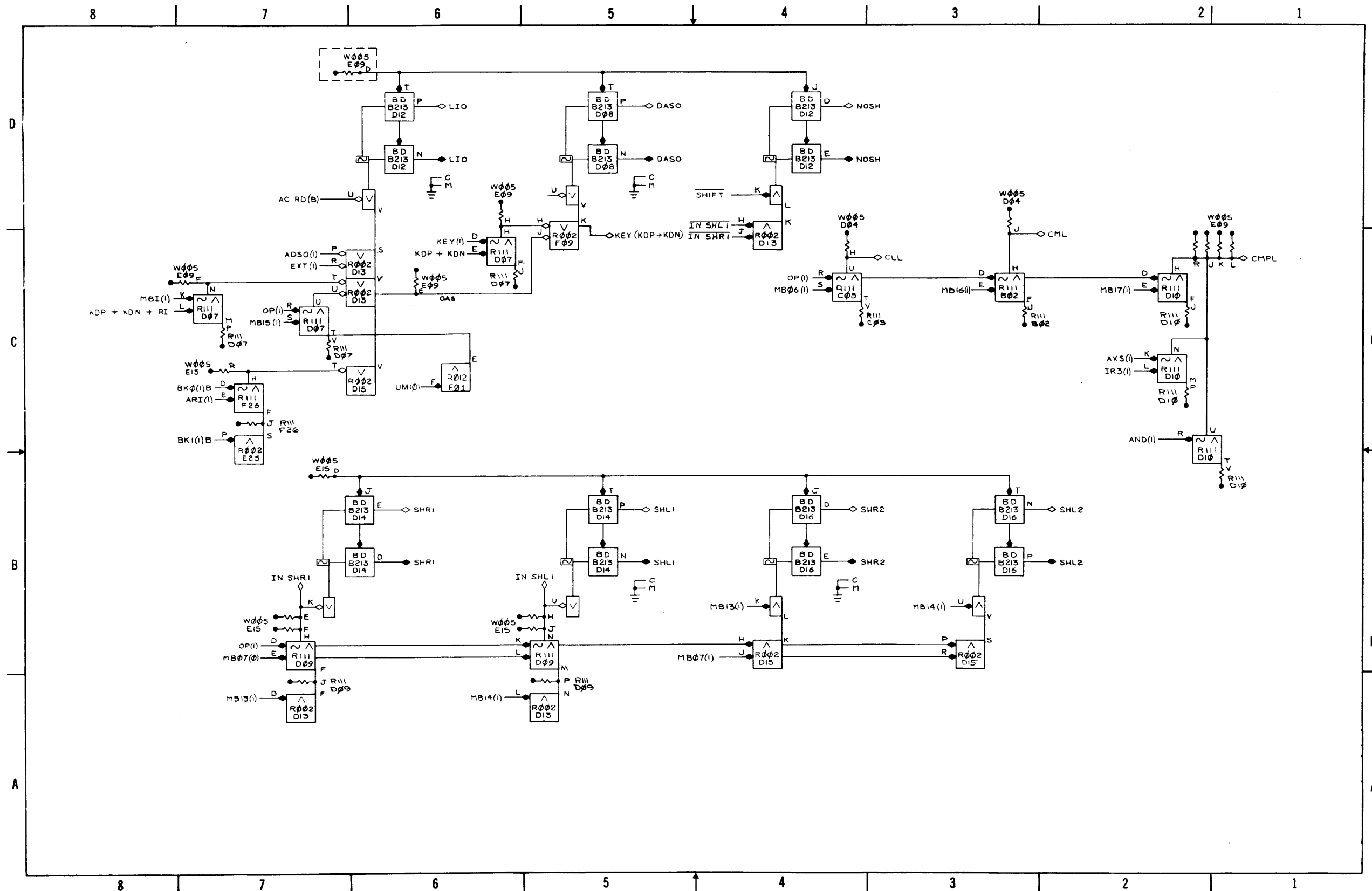
D-BS-KC09-C-10 Clock and Run and Display



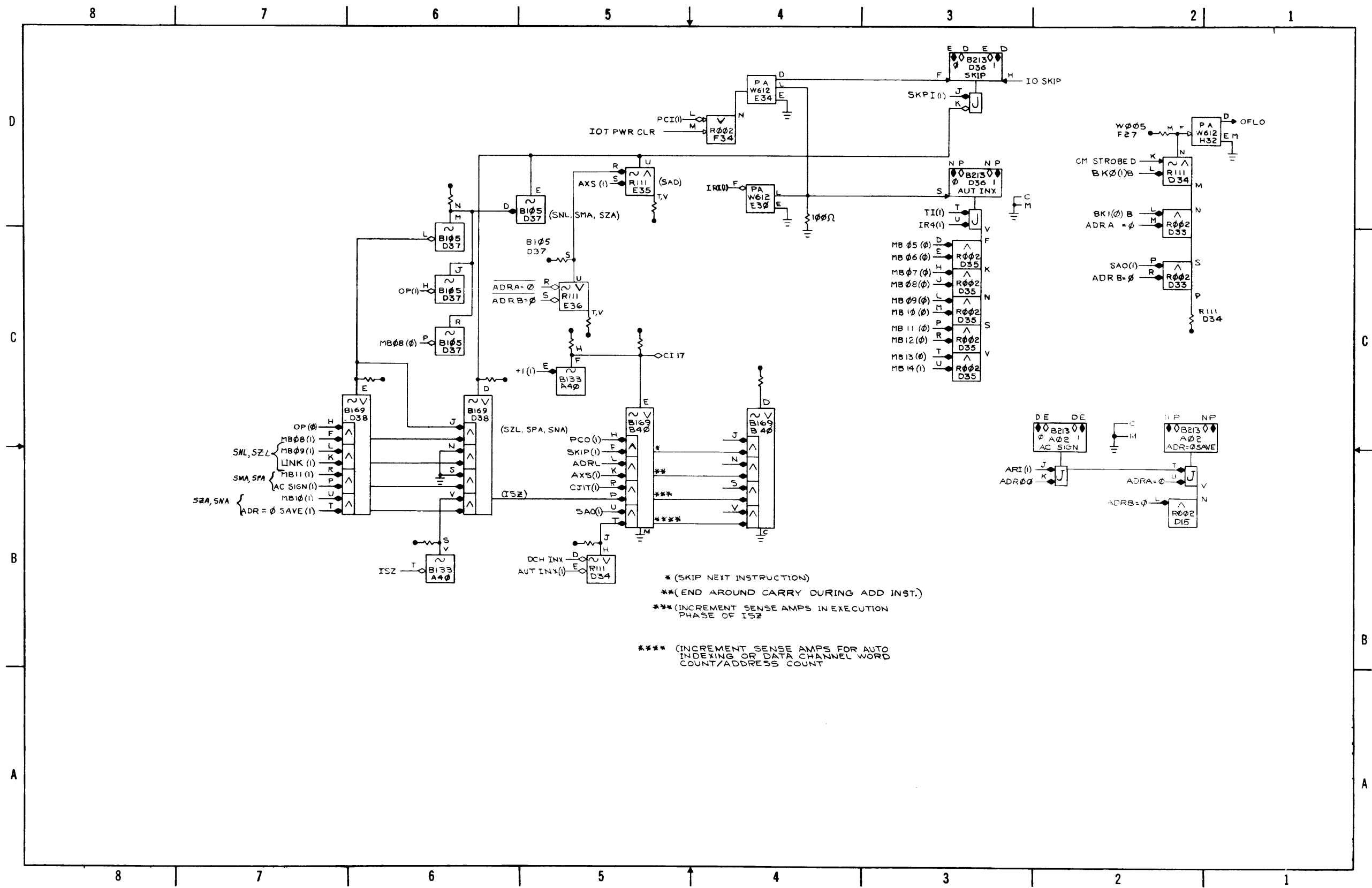
D-TD-KC09-C-11 Clock and Run and Display Timing Diagram



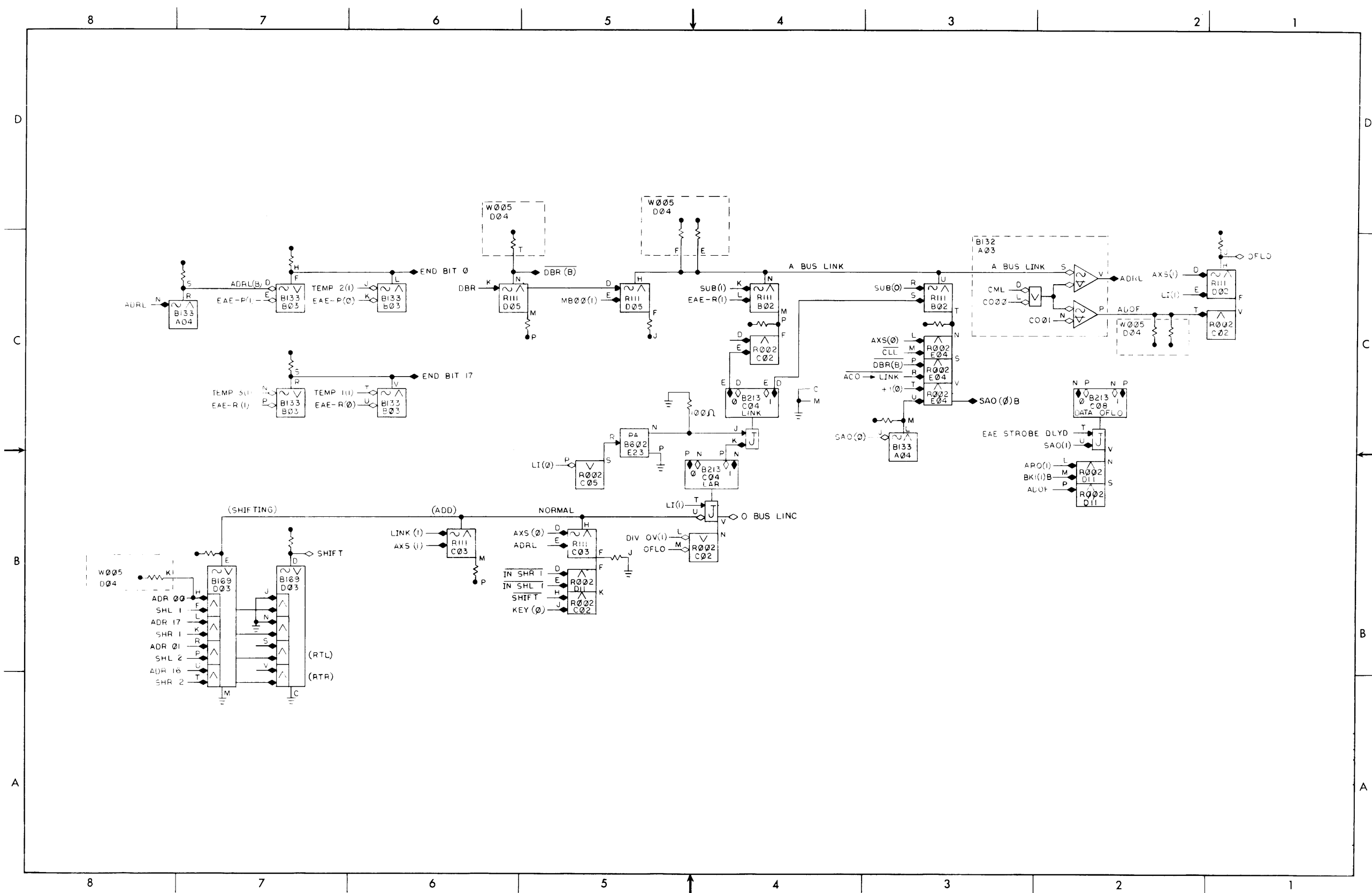
D-BS-KC09-C-12 IR



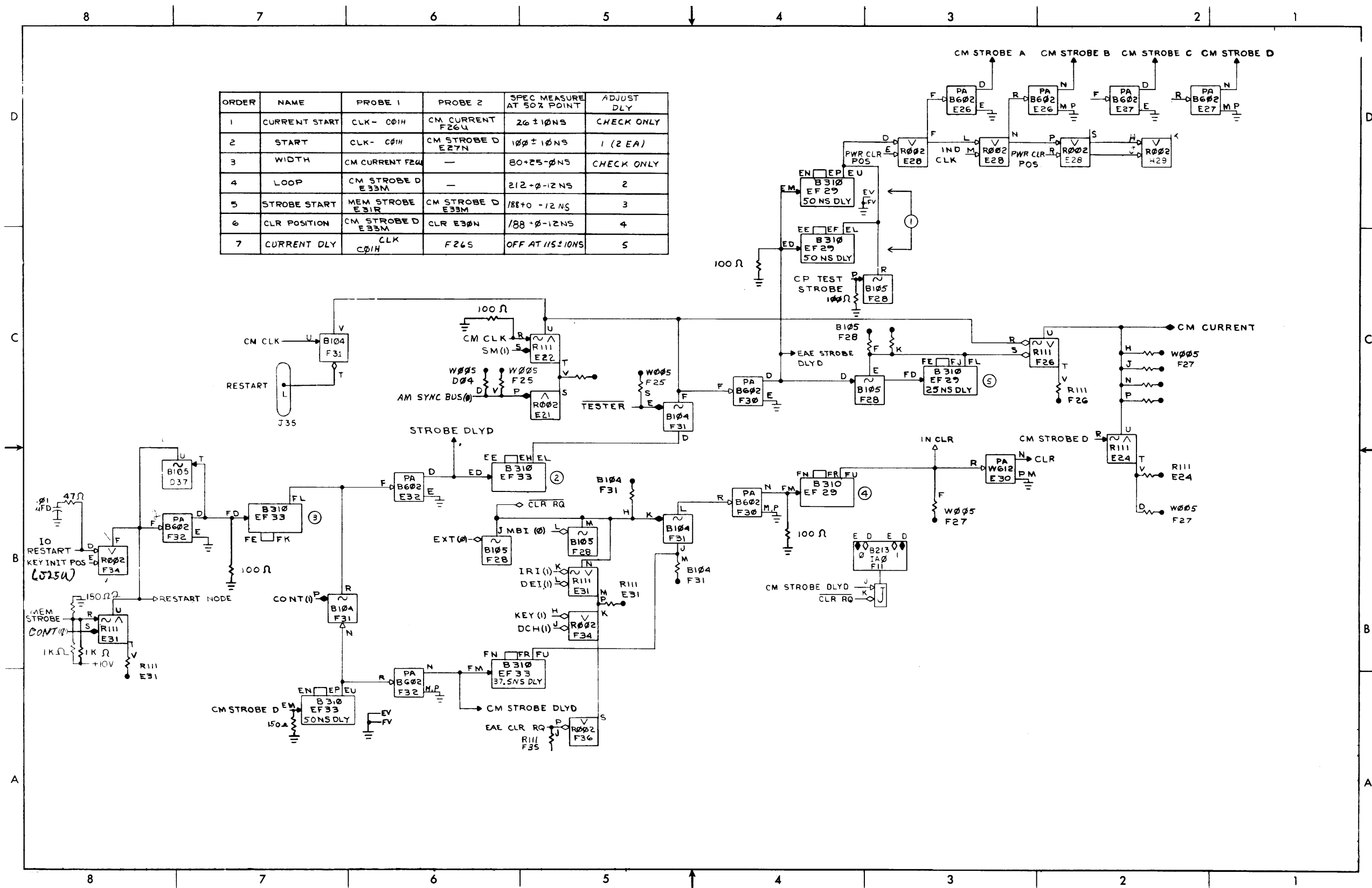
D-BS-KC09-C-13 Operate Control



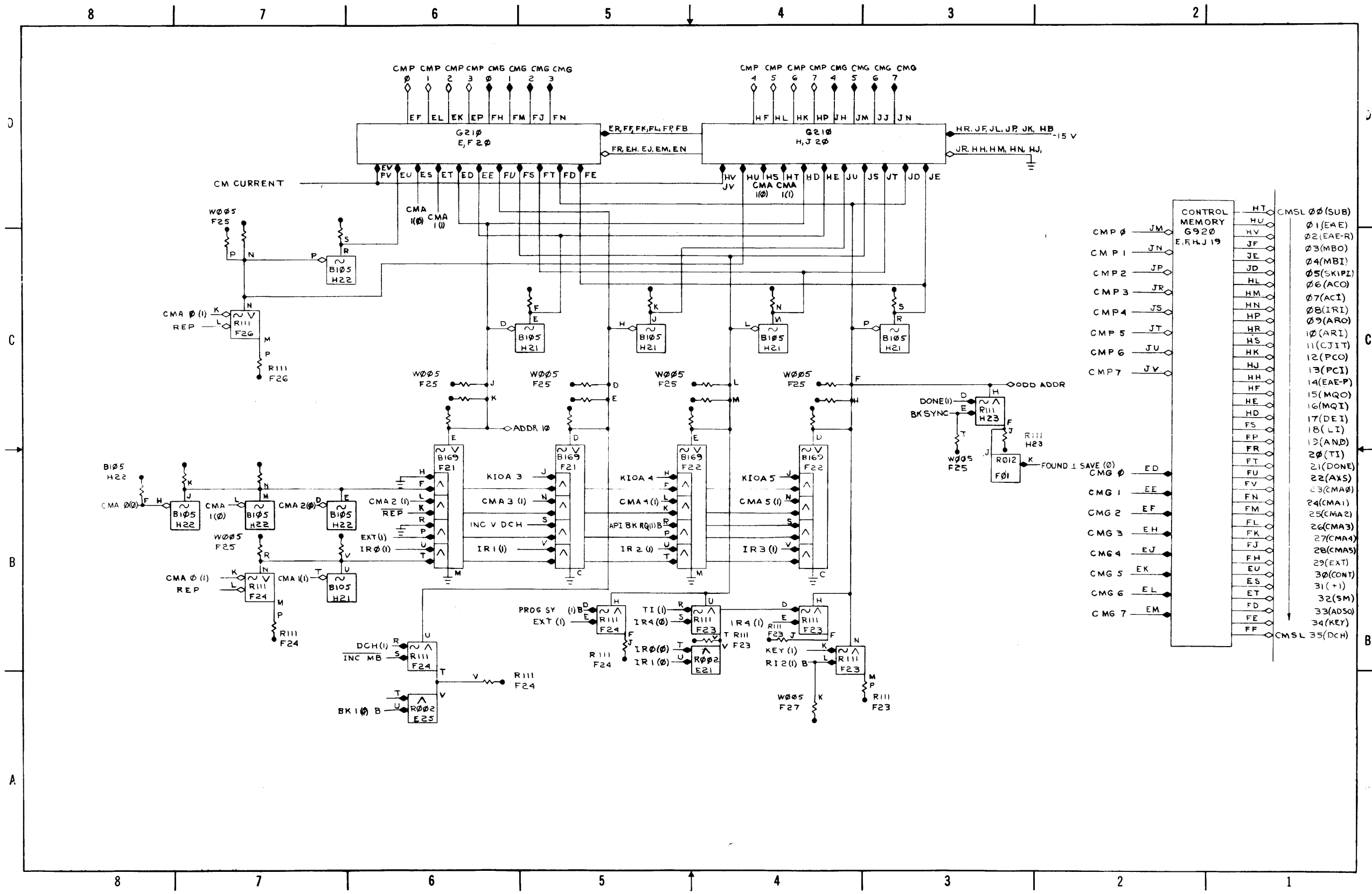
D-BS-KC09-C-14 SKIP and CI17



D-BS-KC09-C-15 Link Control

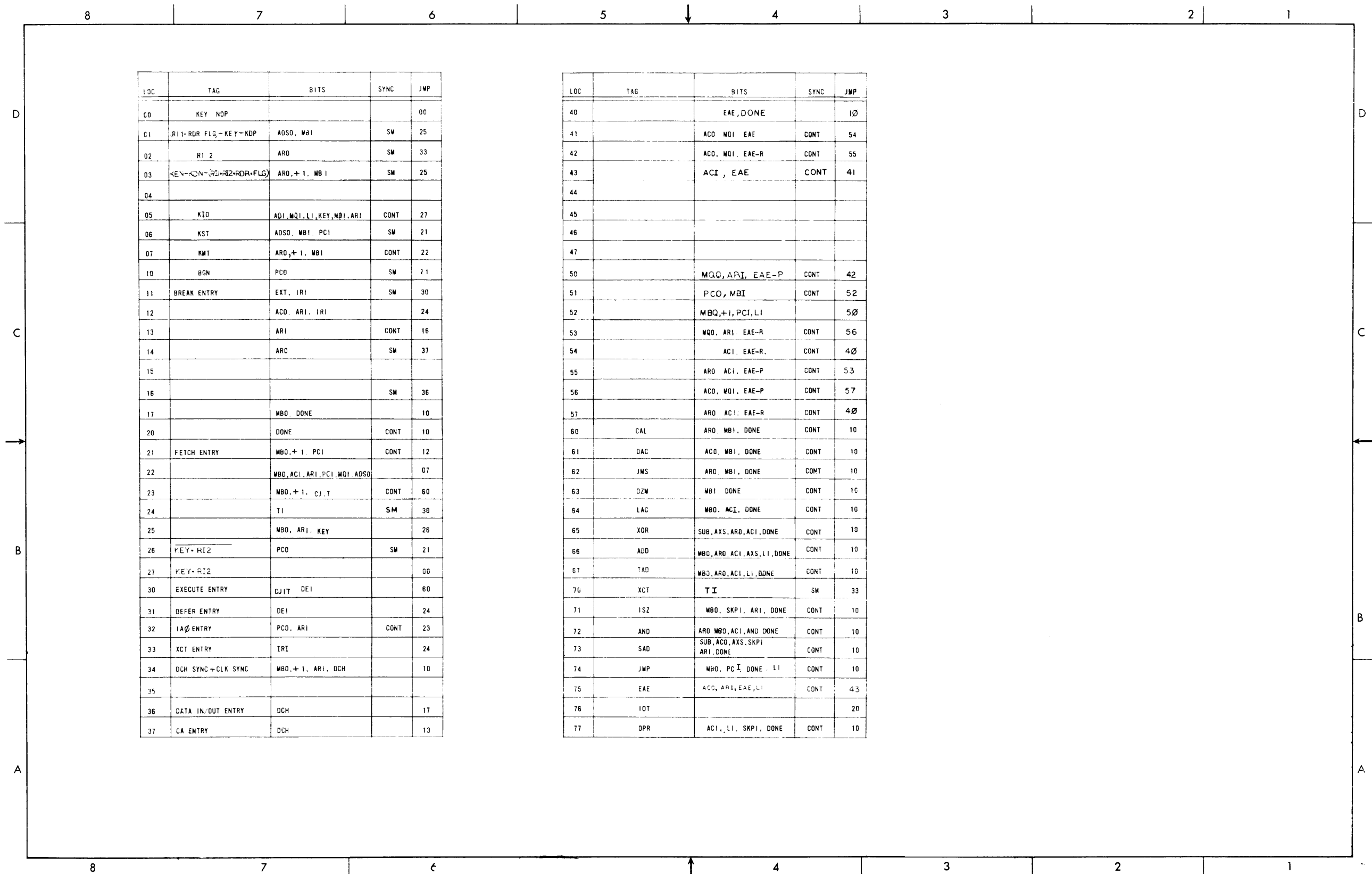


D-BS-KC09-C-16 CM Timing



Control Memory (G920)	Control Memory (G210)	Control Memory (CMG)	Control Memory (CMP)
HT	HT	CMG 0	CMP 0
HU	HU	CMG 1	CMP 1
HV	HV	CMG 2	CMP 2
JF	JF	CMG 3	CMP 3
JE	JE	CMG 4	CMP 4
JD	JD	CMG 5	CMP 5
HL	HL	CMG 6	CMP 6
HM	HM	CMG 7	CMP 7
HN	HN		
HP	HP		
HR	HR		
HS	HS		
HK	HK		
HJ	HJ		
HH	HH		
HF	HF		
HE	HE		
HD	HD		
FS	FS		
FP	FP		
FR	FR		
FT	FT		
FV	FV		
FN	FN		
FM	FM		
FL	FL		
FK	FK		
FJ	FJ		
FE	FE		
ED	ED		
EU	EU		
ES	ES		
ET	ET		
ET	ET		
FD	FD		
FE	FE		
FF	FF		

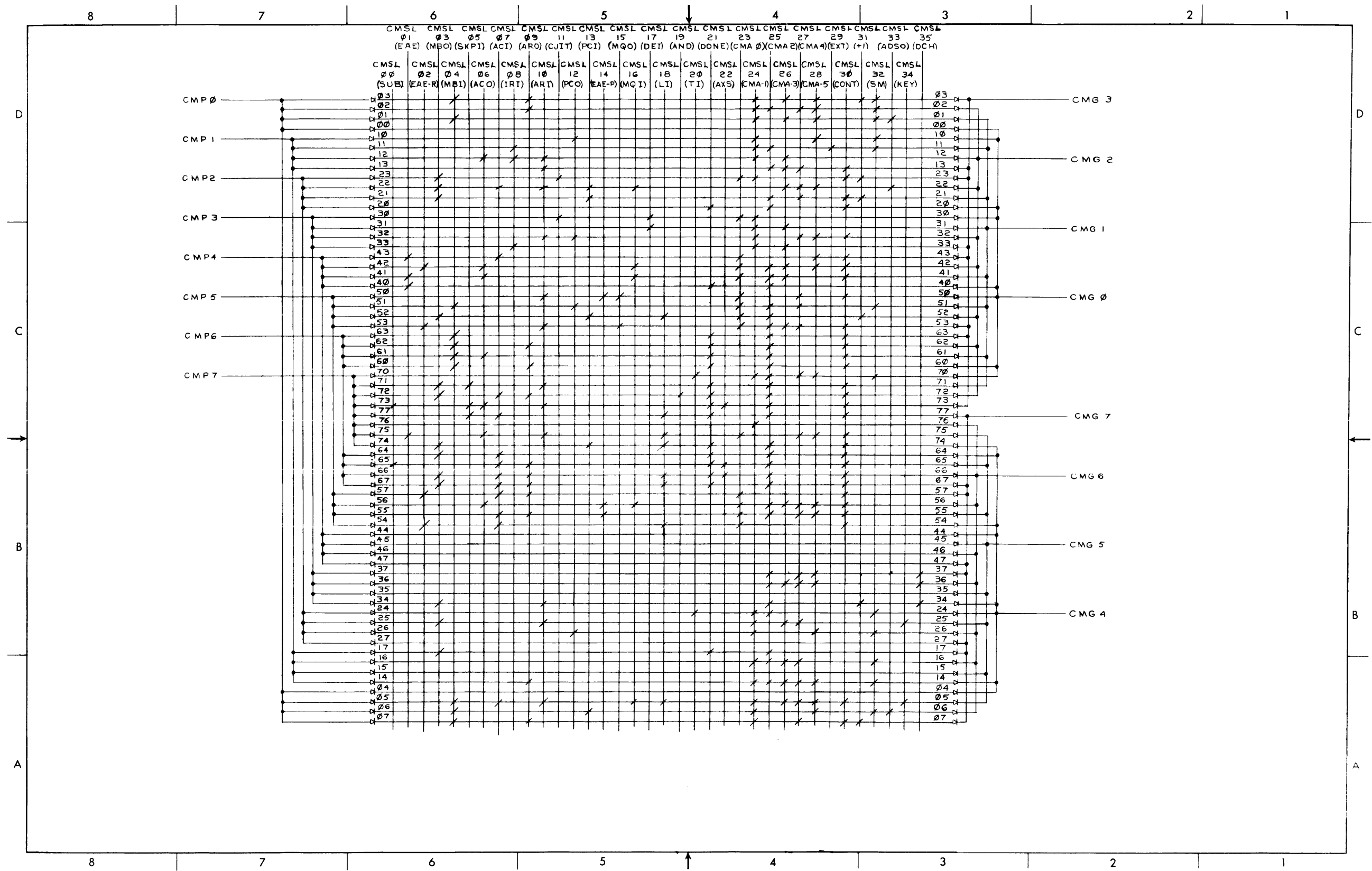
D-BS-KC09-C-17 CM Addressing



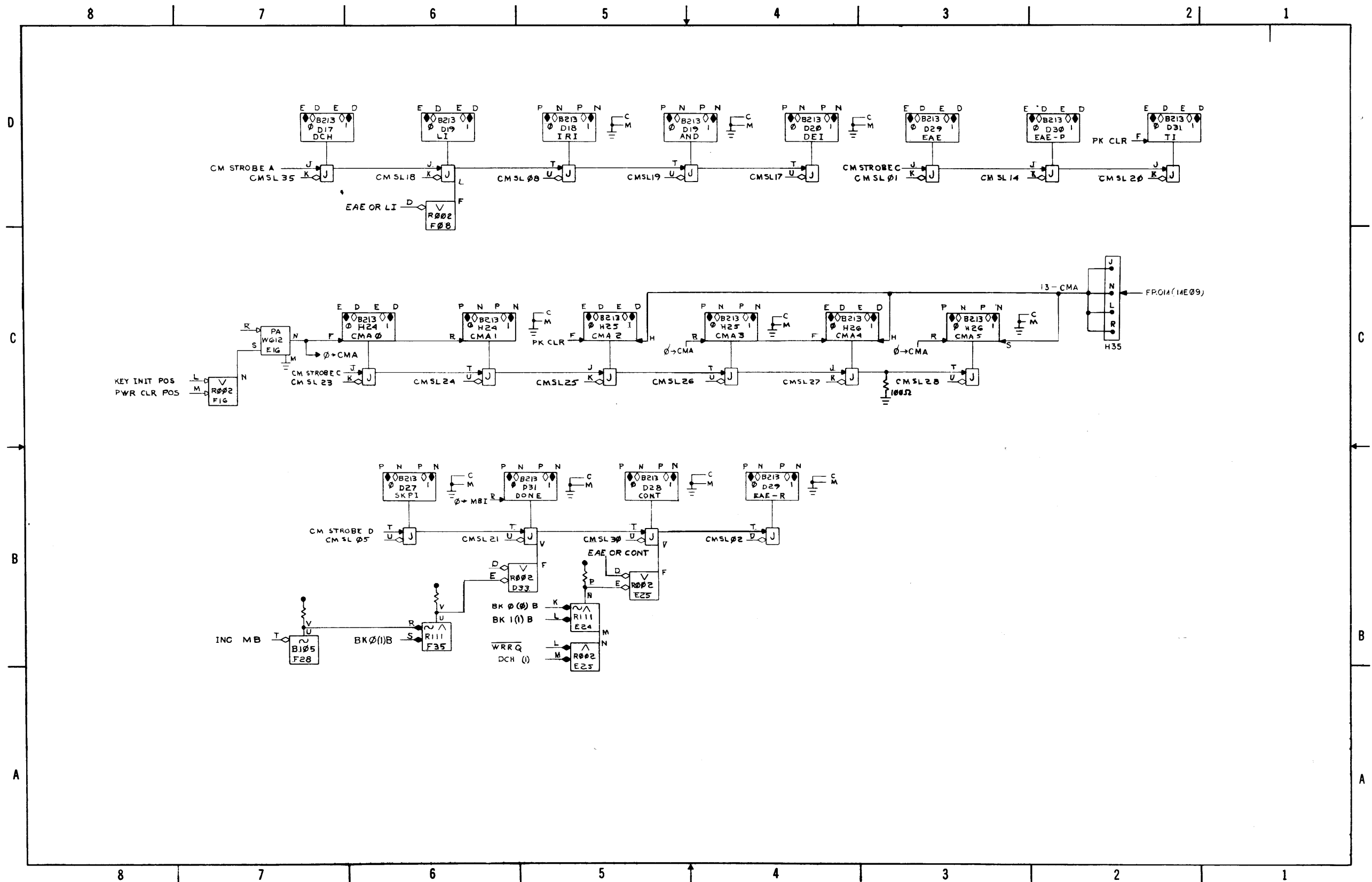
LOC	TAG	BITS	SYNC	JMP
00	KEY NDP			00
01	RI1-RDR FLG-KEY-KDP	ADSO, MBI	SM	25
02	RI 2	ARO	SM	33
03	KEY-CON-RI1-RI2-RDR-FLG	ARO,+1, MBI	SM	25
04				
05	KIO	AOI, MQI, LI, KEY, MBI, ARI	CONT	27
06	KST	ADSO, MBI, PCI	SM	21
07	KMT	ARO,+1, MBI	CONT	22
10	BGN	PCO	SM	21
11	BREAK ENTRY	EXT, IRI	SM	30
12		ACO, ARI, IRI		24
13		ARI	CONT	16
14		ARO	SM	37
15				
16			SM	36
17		MBO, DONE		10
20		DONE	CONT	10
21	FETCH ENTRY	MBO,+1, PCI	CONT	12
22		MBO, ACI, ARI, PCI, MQI, ADSO		07
23		MBO,+1, CJ, T	CONT	60
24		TI	SM	30
25		MBO, ARI, KEY		26
26	KEY-RI2	PCO	SM	21
27	KEY-RI2			00
30	EXECUTE ENTRY	CJIT, DEI		60
31	DEFER ENTRY	DEI		24
32	IAØ ENTRY	PCO, ARI	CONT	23
33	XCT ENTRY	IRI		24
34	DCH SYNC+CLK SYNC	MBO,+1, ARI, DCH		10
35				
36	DATA IN/OUT ENTRY	DCH		17
37	CA ENTRY	DCH		13

LOC	TAG	BITS	SYNC	JMP
40		EAE, DONE		10
41		ACO, MQI, EAE	CONT	54
42		ACO, MQI, EAE-R	CONT	55
43		ACI, EAE	CONT	41
44				
45				
46				
47				
50		MQO, API, EAE-P	CONT	42
51		PCO, MBI	CONT	52
52		MBQ,+1, PCI, LI		50
53		MQO, ARI, EAE-R	CONT	56
54		ACI, EAE-R	CONT	40
55		ARO, ACI, EAE-P	CONT	53
56		ACO, MQI, EAE-P	CONT	57
57		ARO, ACI, EAE-R	CONT	40
60	CAL	ARO, MBI, DONE	CONT	10
61	DAC	ACO, MBI, DONE	CONT	10
62	JMS	ARO, MBI, DONE	CONT	10
63	DZM	MBI, DONE	CONT	10
64	LAC	MBO, ACI, DONE	CONT	10
65	XDR	SUB, AXS, ARO, ACI, DONE	CONT	10
66	ADD	MBO, ARO, ACI, AXS, LI, DONE	CONT	10
67	TAD	MBO, ARO, ACI, LI, DONE	CONT	10
70	XCT	TI	SM	33
71	ISZ	MBO, SKPI, ARI, DONE	CONT	10
72	AND	ARO, MBO, ACI, AND, DONE	CONT	10
73	SAD	SUB, ACO, AXS, SKPI, ARI, DONE	CONT	10
74	JMP	MBO, PCI, DONE, LI	CONT	10
75	EAE	ACO, ARI, EAE, LI	CONT	43
76	IOT			20
77	OPR	ACI, LI, SKPI, DONE	CONT	10

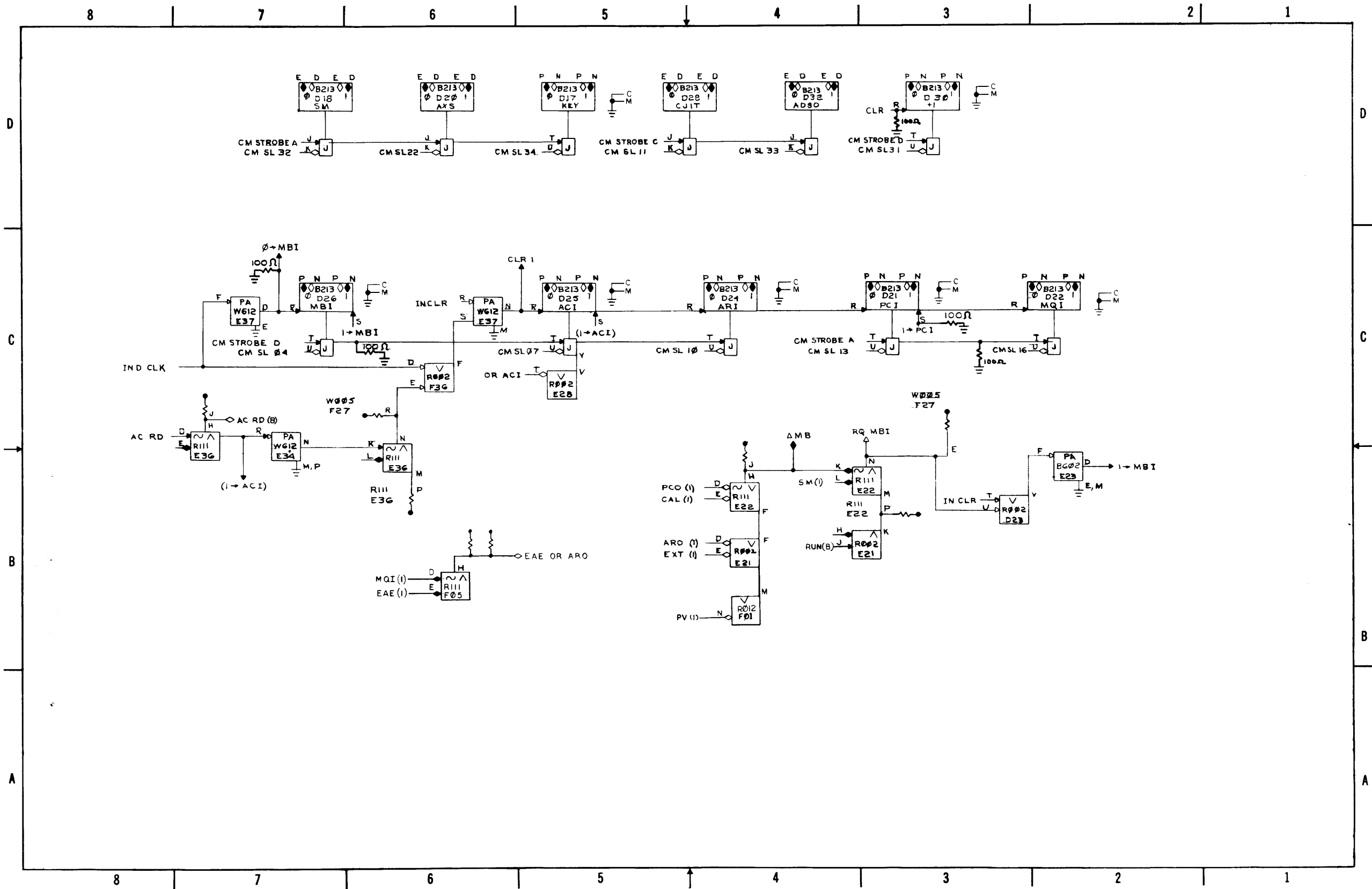
D-FD-KC09-C-18 CM Wiring Matrix and Program (Sheet 1)



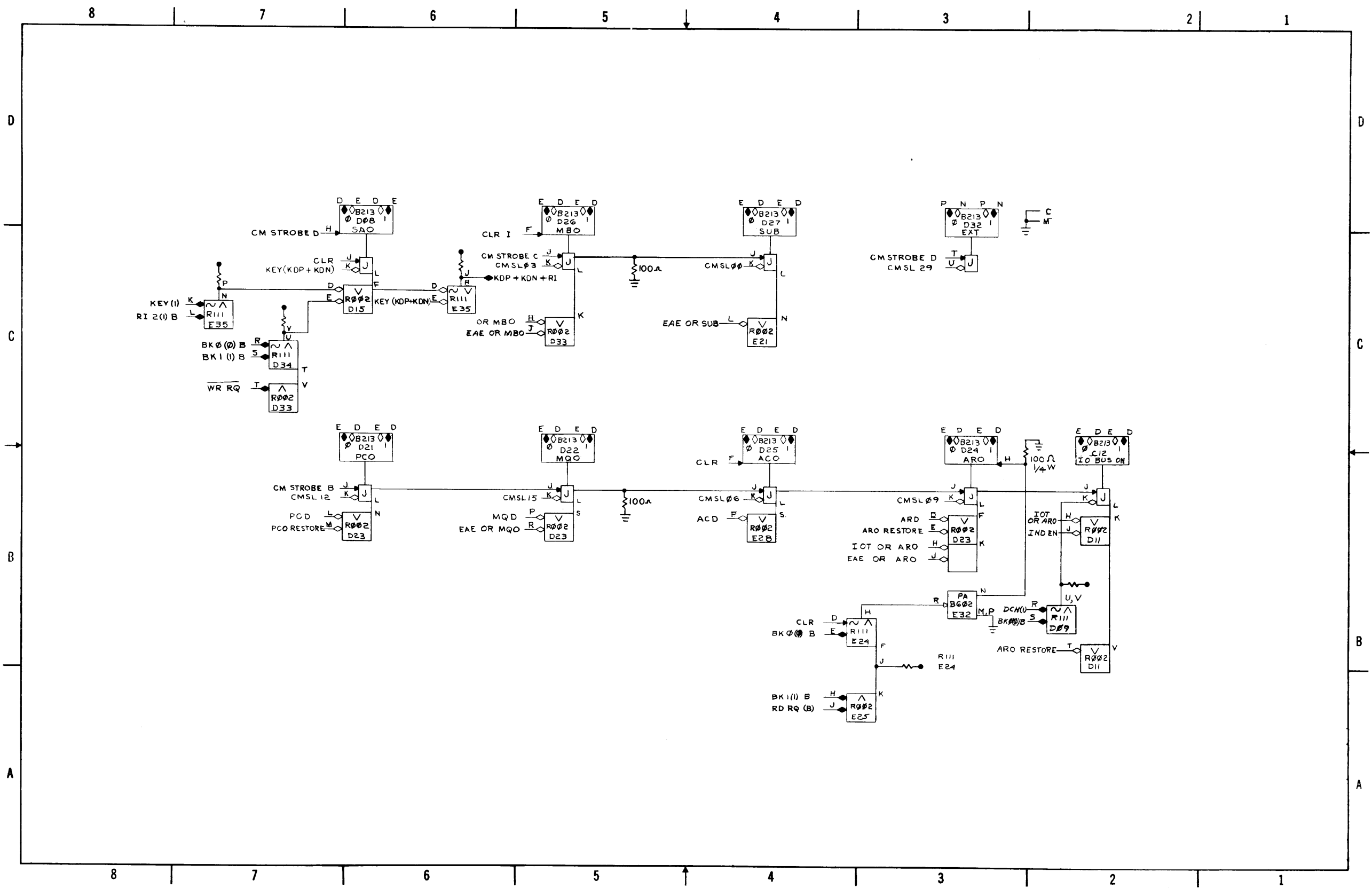
D-FD-KC09-C-18 CM Wiring Matrix and Program (Sheet 2)



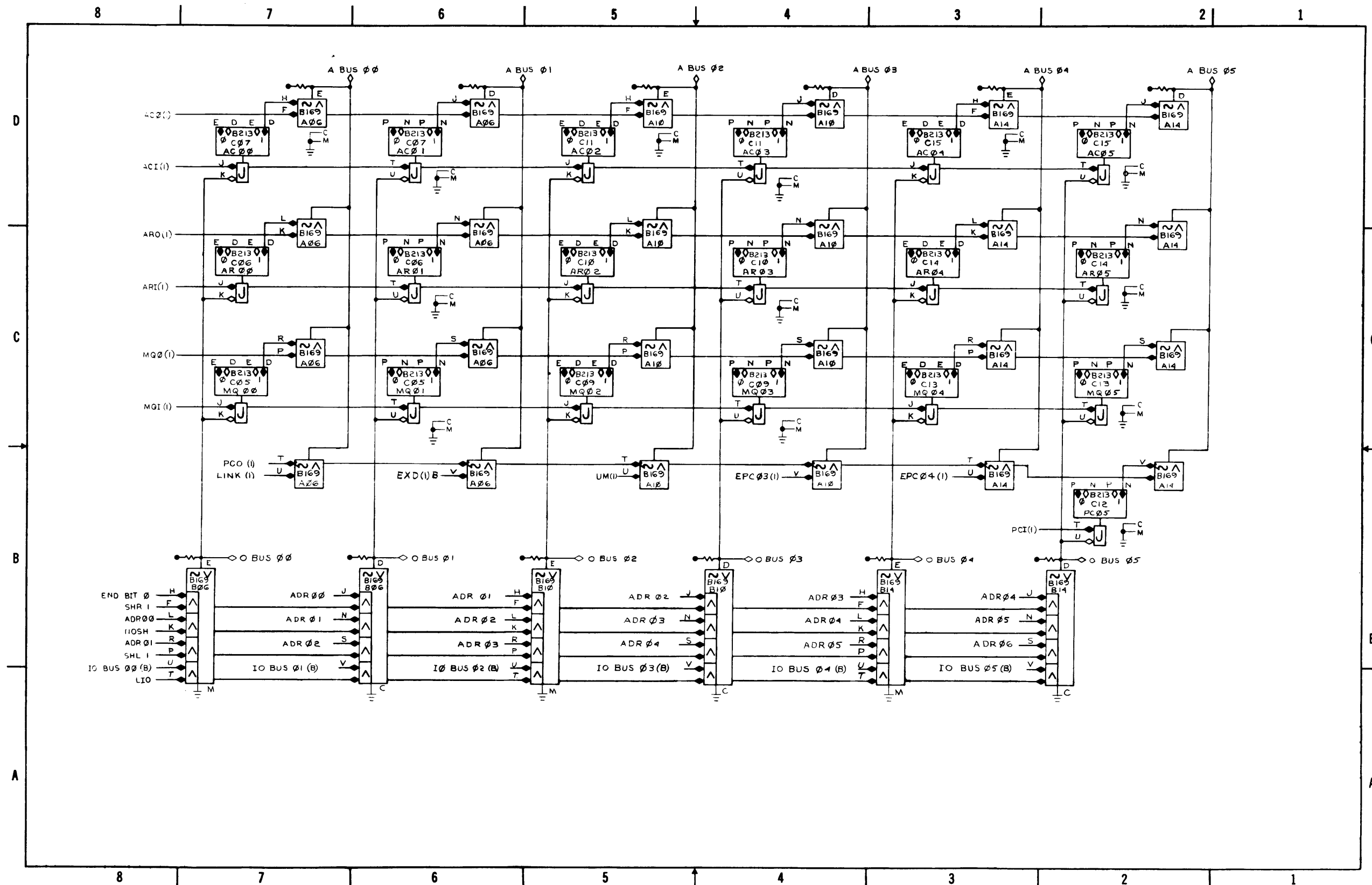
D-BS-KC09-C-19 CM Sense Flops (Sheet 1)



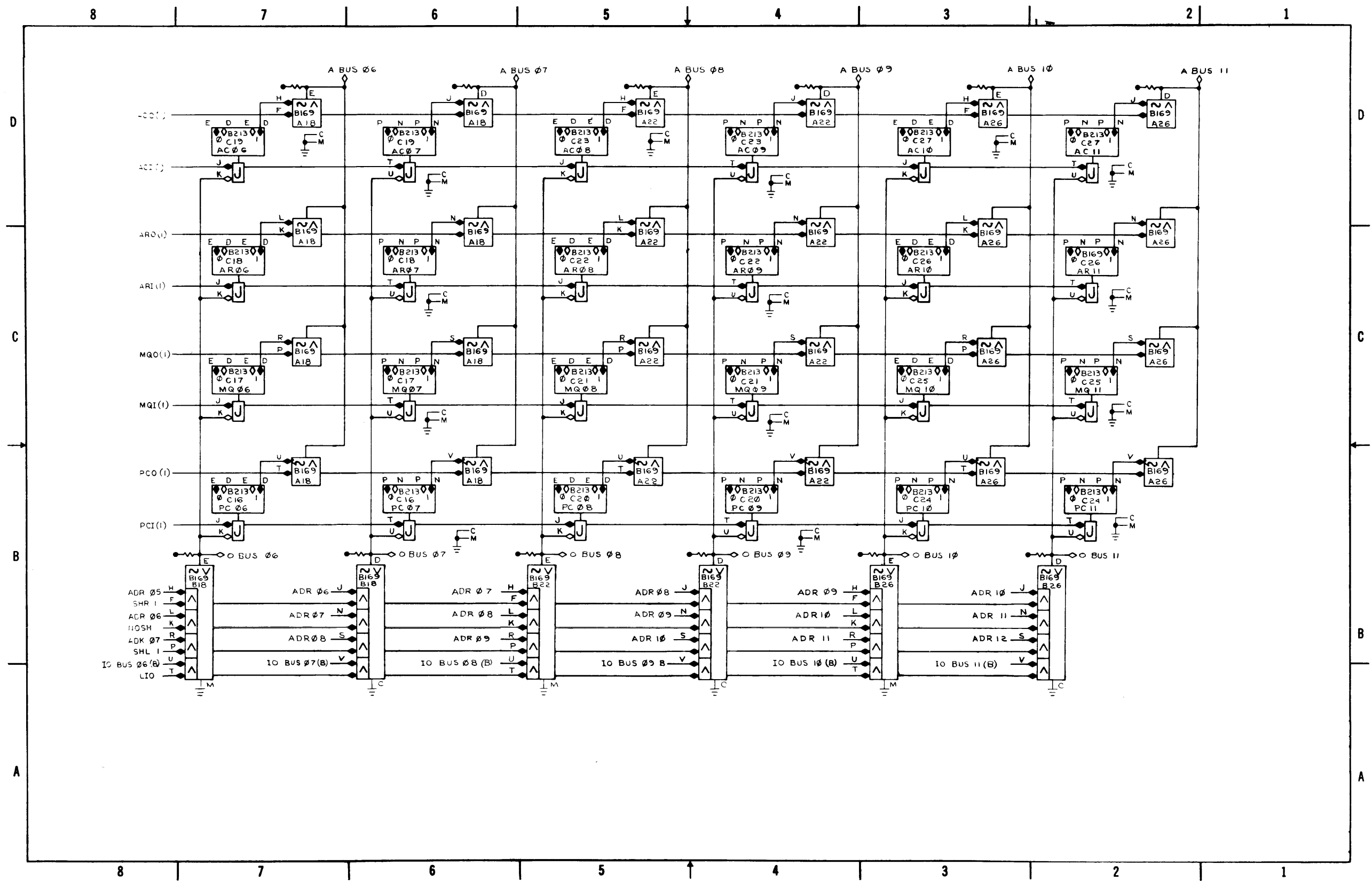
D-BS-KC09-C-19 CM Sense Flops (Sheet 2)



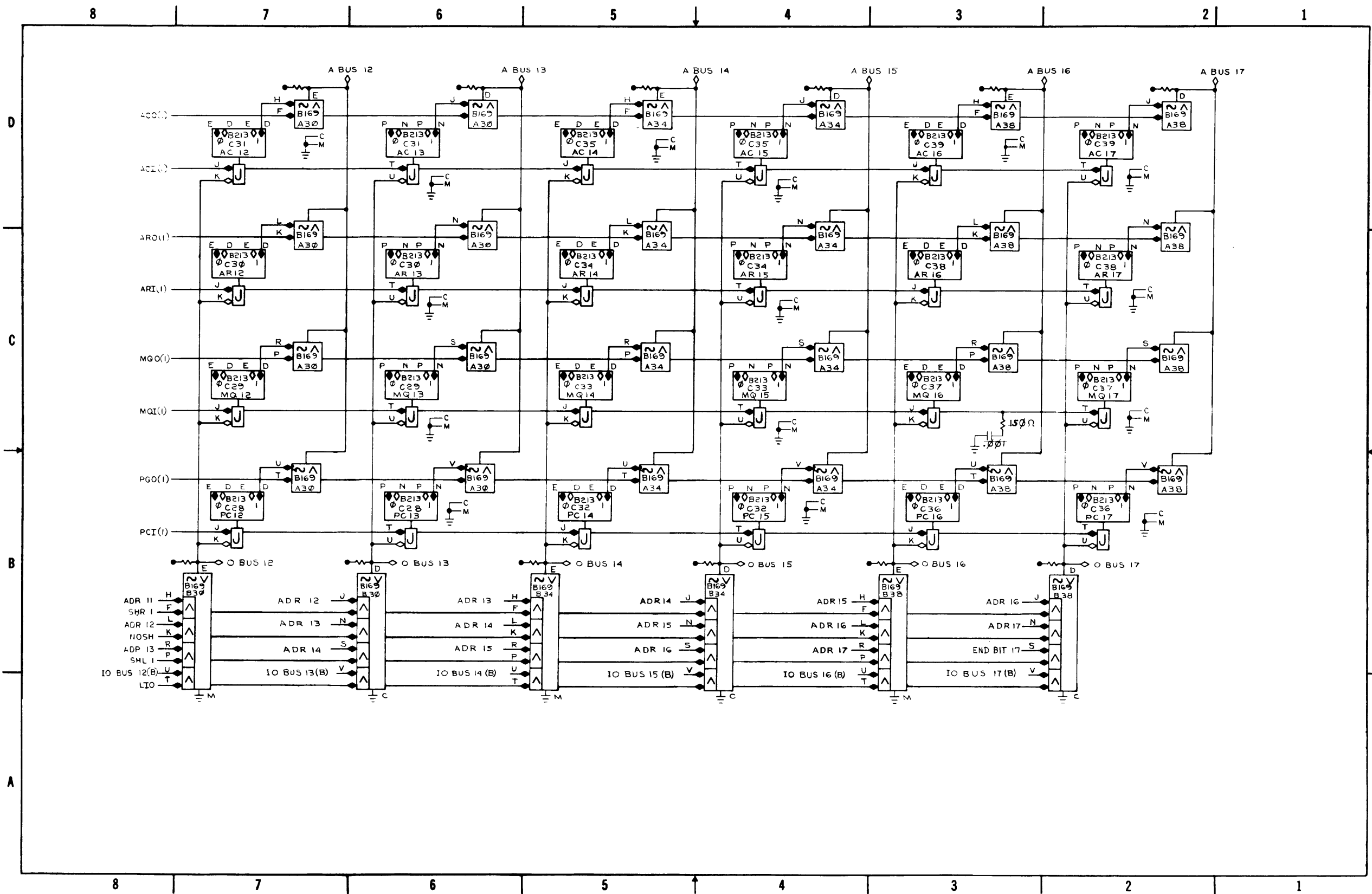
D-BS-KC09-C-19 CM Sense Flops (Sheet 3)



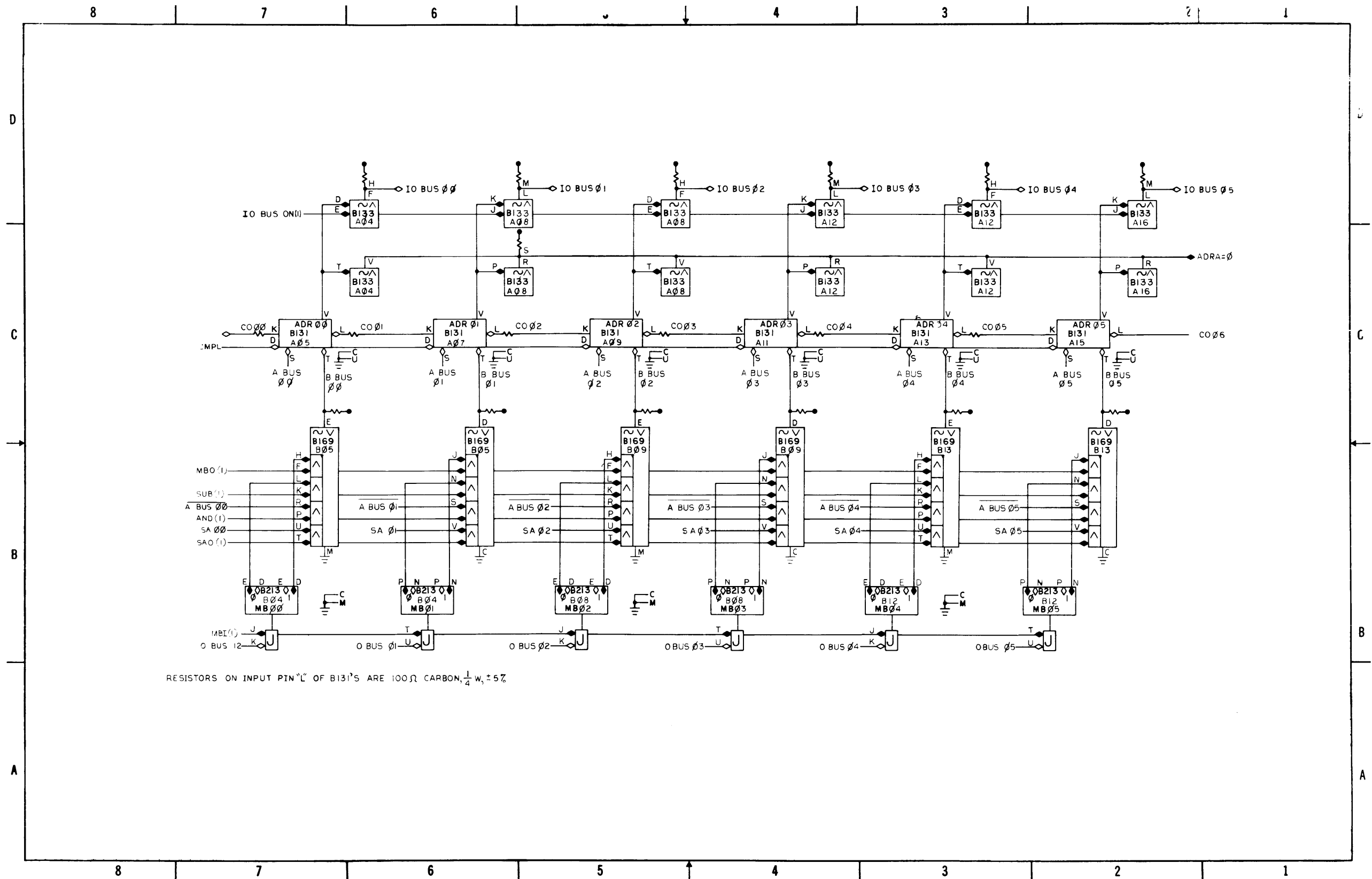
D-BS-KC09-C-20 AC, AR, MC, PC (Sheet 1)



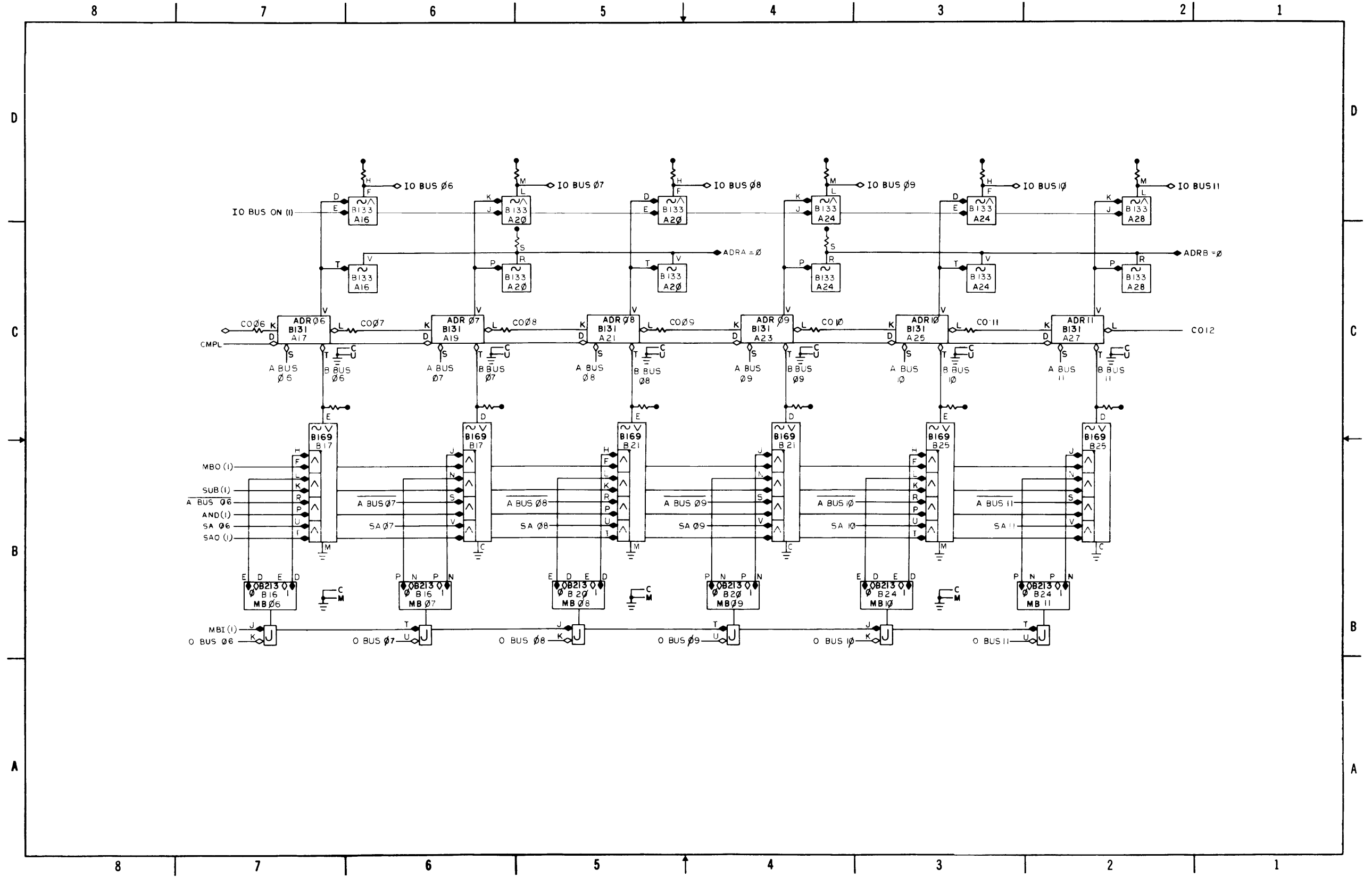
D-BS-KC09-C-20 AC, AR, MC, PC (Sheet 2)



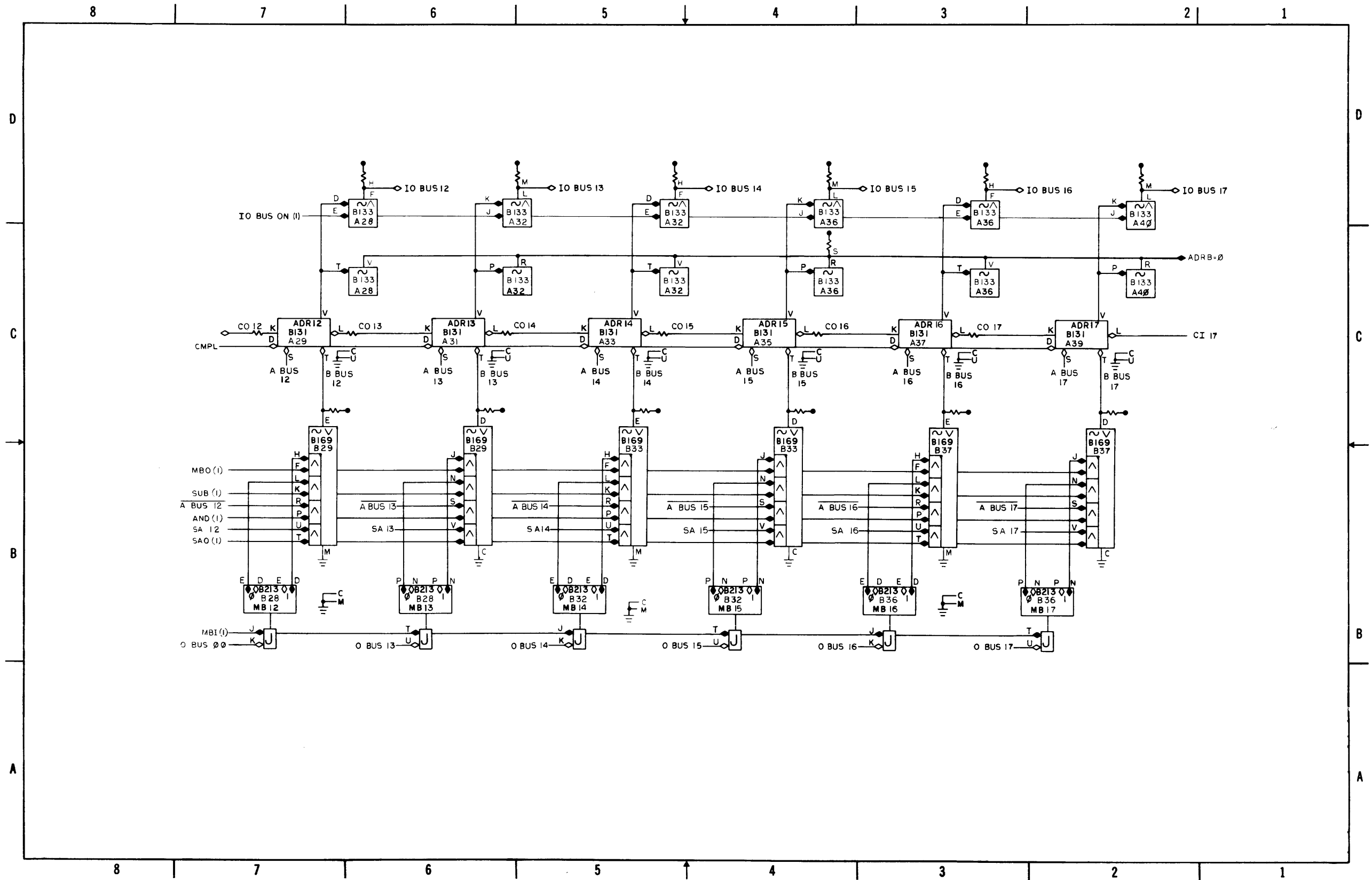
D-BS-KC09-C-20 AC, AR, MC, PC (Sheet 3)



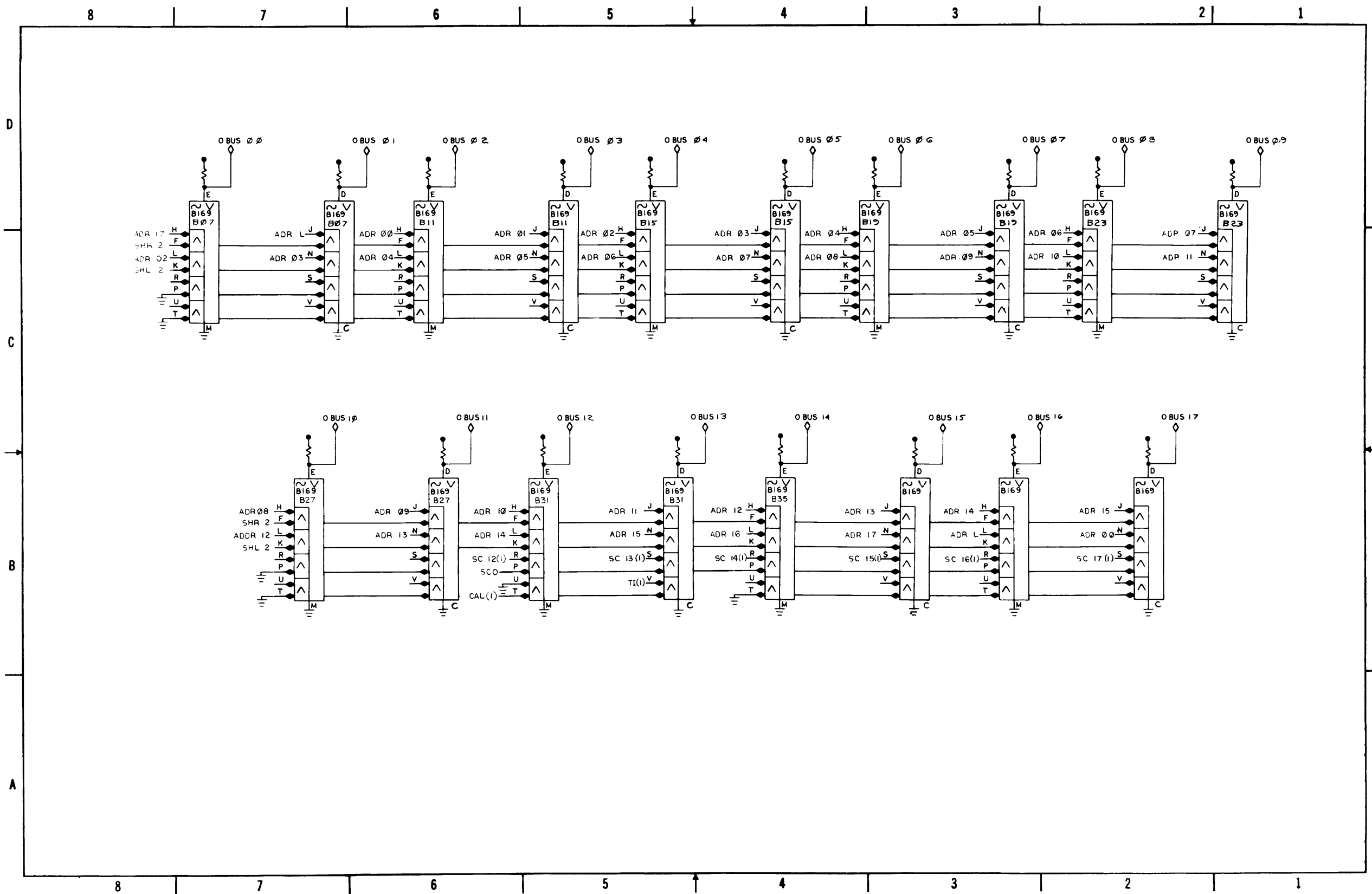
D-BS-KC09-C-21 MB and Adder (Sheet 1)



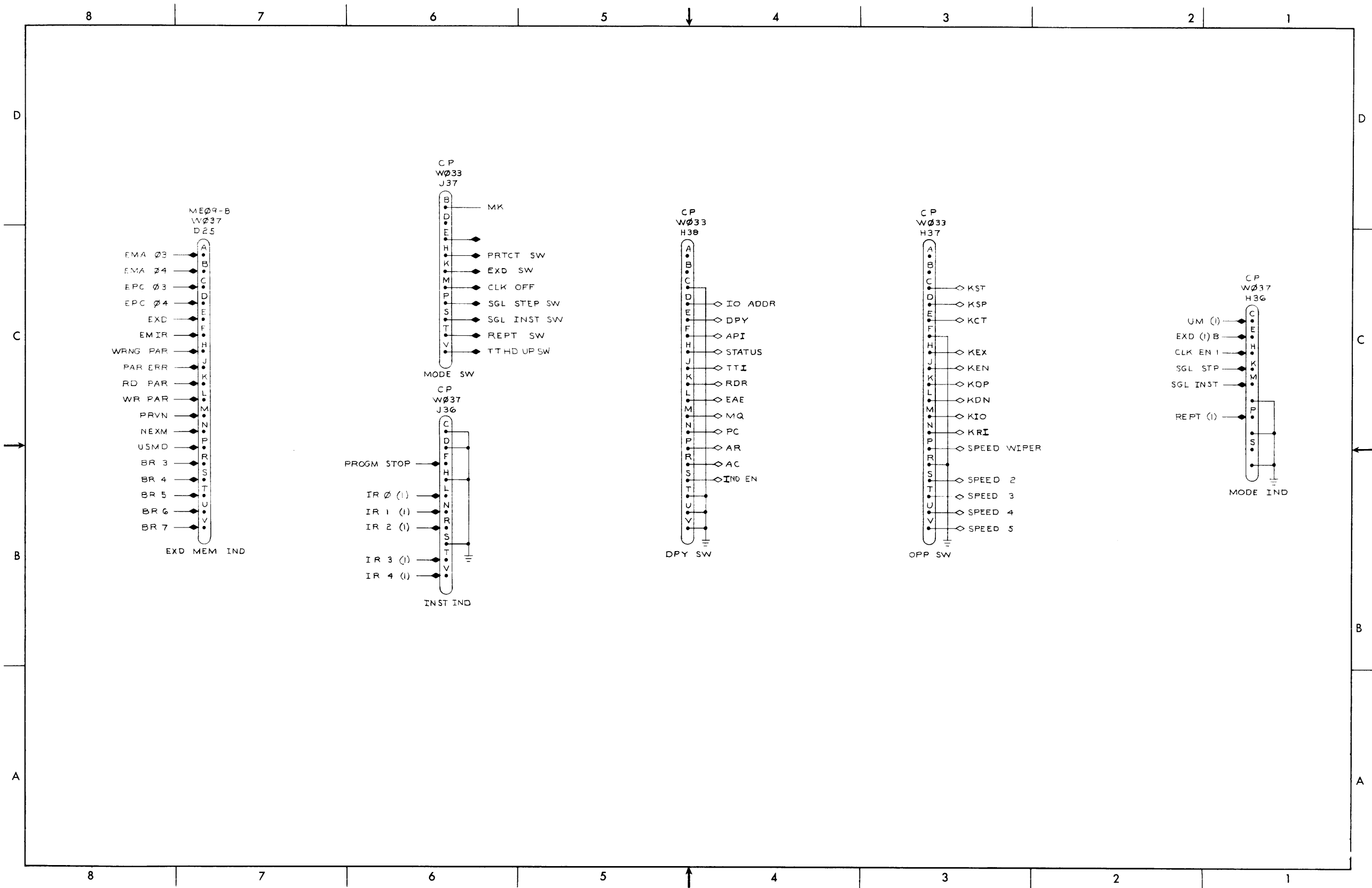
D-BS-KC09-C-21 MB and Adder (Sheet 2)



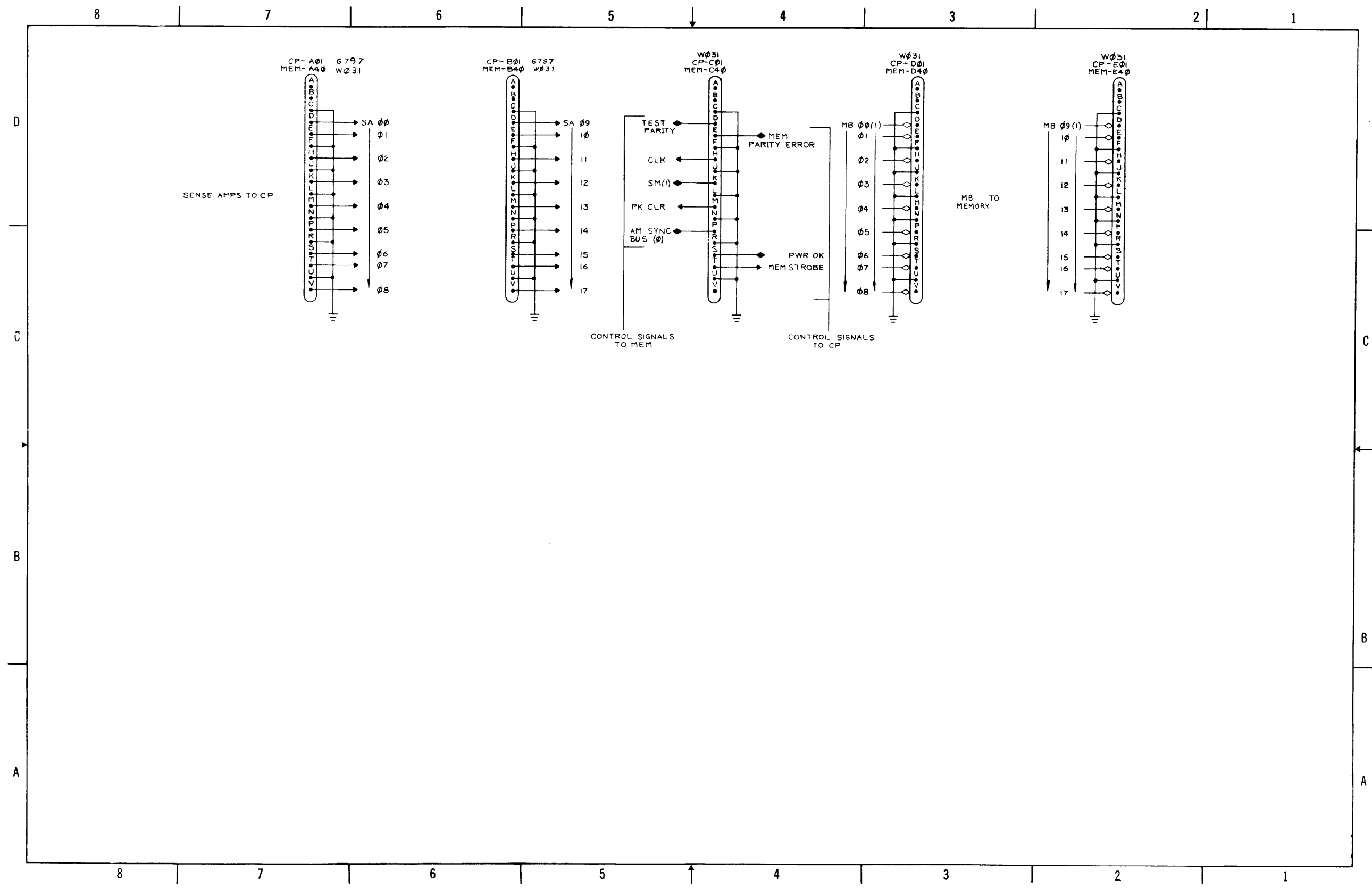
D-BS-KC09-C-21 MB and Adder (Sheet 3)



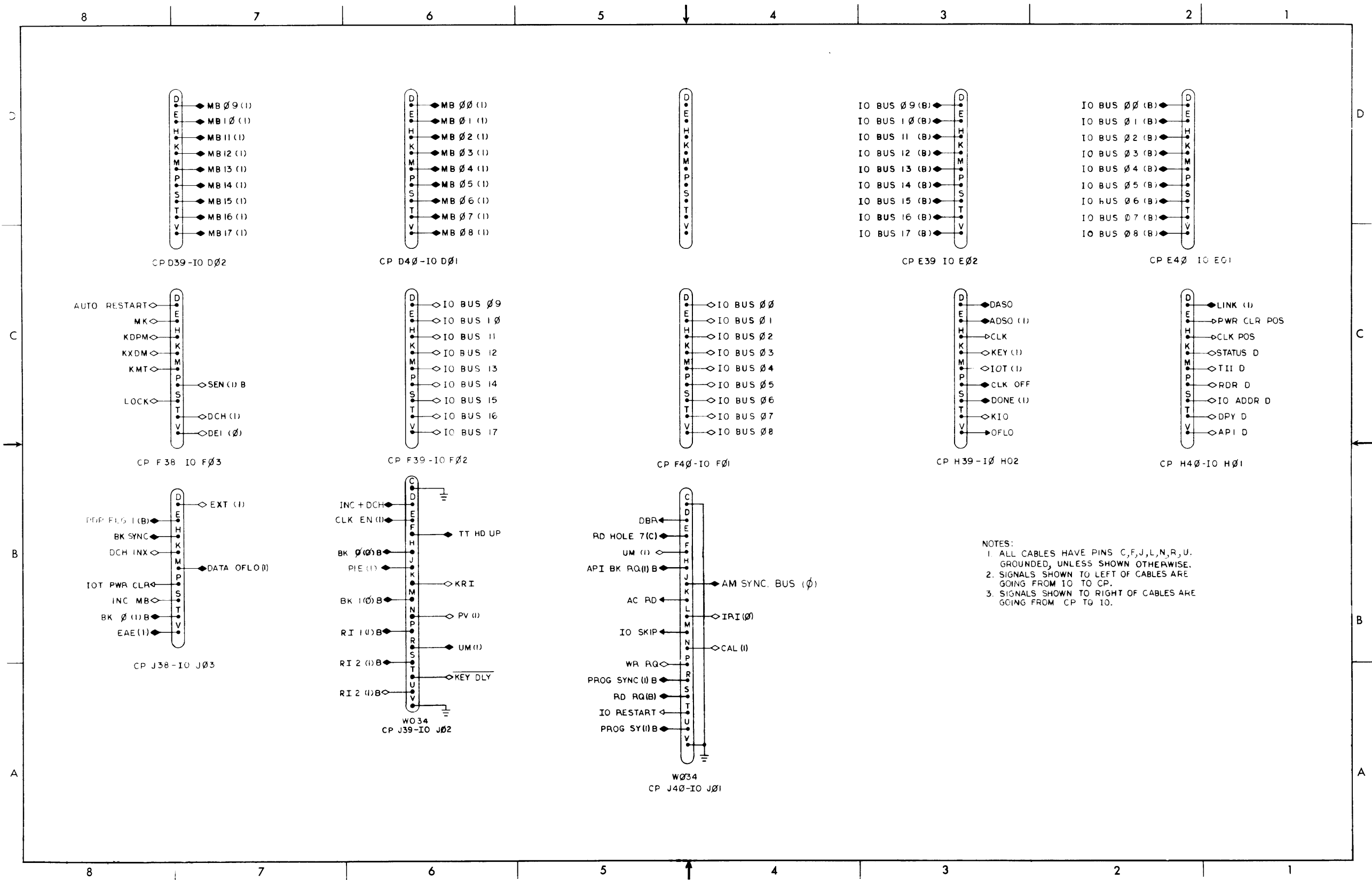
D-BS-KC09-C-22 Shift X2 Gates



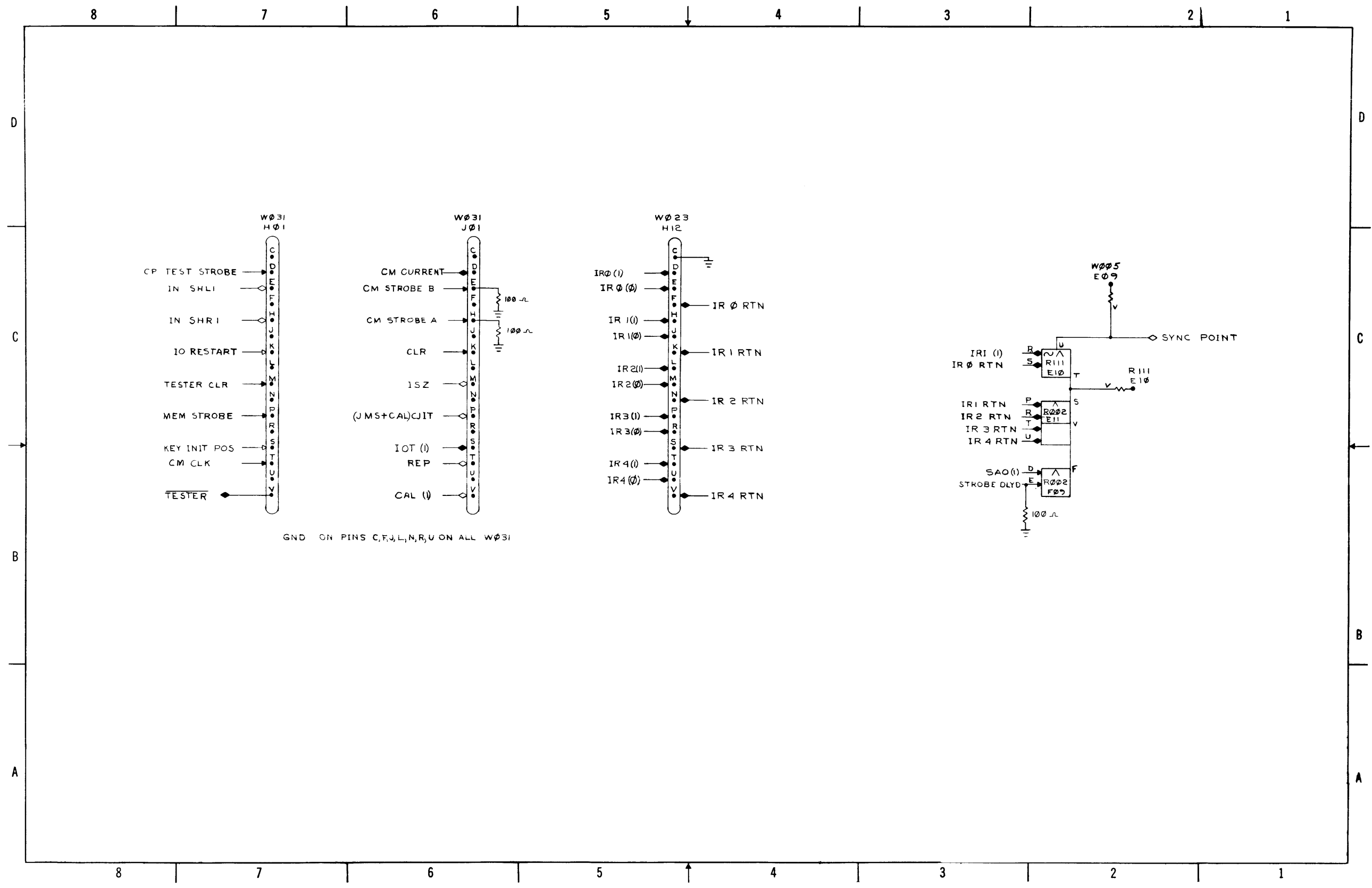
D-IC-KC09-C-23 CP - Console Interface



D-IC-KC09-C-24 CP - Memory Interface



D-IC-KC09-C-25 CP-IO Cable Interface



D-BS-KC09-C-26 CP Tester Interface

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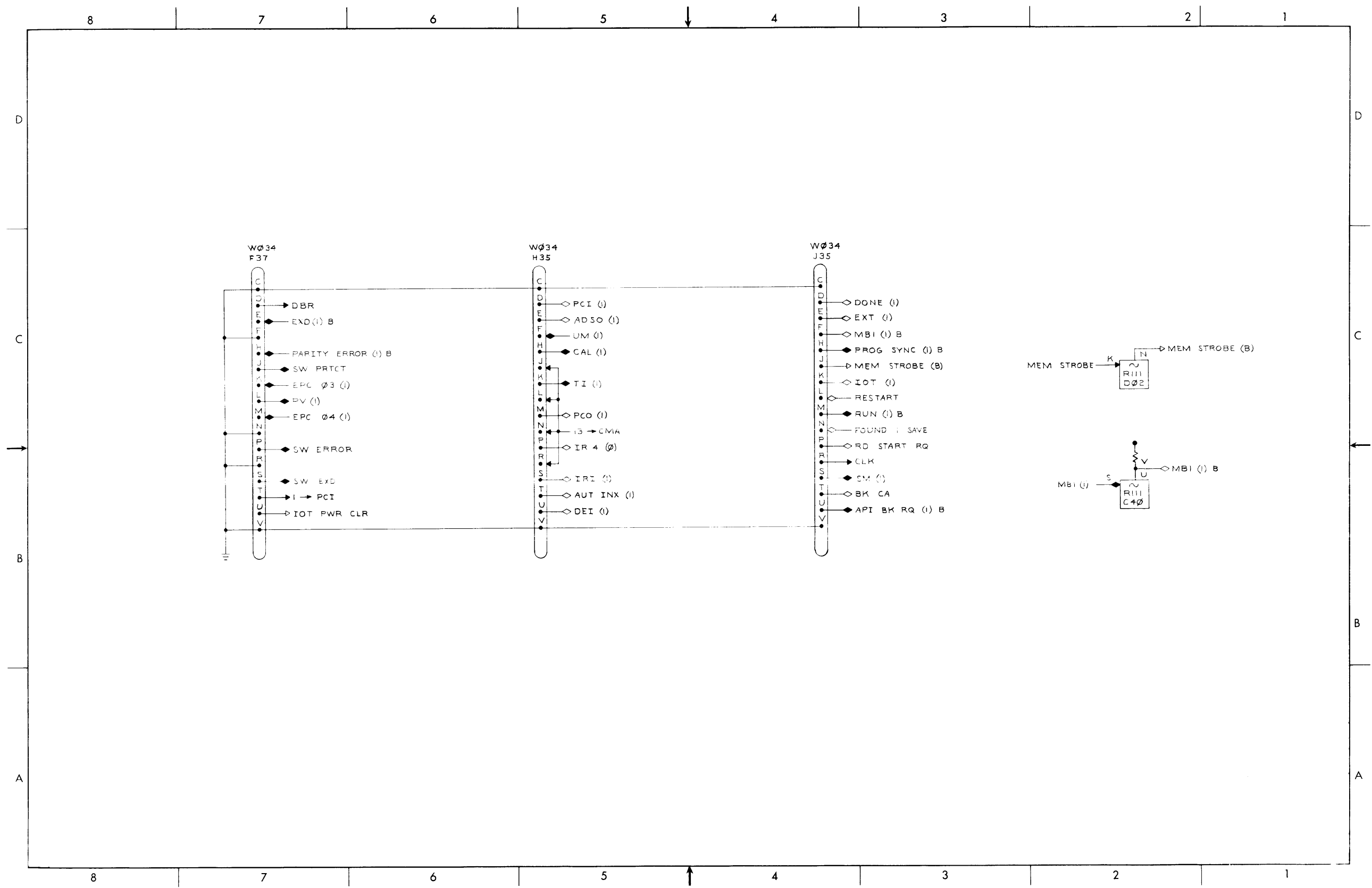
COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
* JUMPER TEMP. 1 (1)	JUMPER		B03T	B03C	
* JUMPER SCO (1)	JUMPER		B31P	B31C	
CM STROBE DLYD	100Ω ½W		F11J	F11C	
CM STROBE D	150Ω ½W		D08H	D08C	
CM STROBE A	100Ω ½W		D22T	D22C	
CM STROBE B	100Ω ½W		D25J	D25C	
CM STROBE C	100Ω ½W		D32J	D32C	
∅ MBI	100Ω ½W		D26R	D27C	
ACI	.001 MFD & 150Ω		J12P	J12C	
F30D	100Ω ½W		E29D	E29C	
CM CLK	100Ω ½W		H01T	H01C	
CM STROBE D	150Ω ½W		E33M	E33C	
STROBE DLYD	100Ω ½W		F09E	F09C	
CP TEST STROBE	100Ω ½W		F28P	F28C	
F30N	100Ω ½W		F29M	F29C	
F32D	100Ω ½W		F33D	F33C	
I/O RESTART	47Ω & .01 MFD		F34D	F34C	
F36N	.010FD 50V		F36N	F36C	
KDPM	15K ½W		F36L	F36B	
LOCK	15K ½W		F36T	F35B	
MEM STROBE	1K ½W		H01P	H01A	
CM STROBE C	100Ω ½W		F15J	F15C	
KMT	15K ½W		H27S	H27B	
CM STROBE B	100Ω ½W		J01E	J02C	
CM STROBE A	100Ω ½W		J01H	J01C	
CLR	100Ω ½W		J01K	H01U	
KXDM RES	15K		J34H	-15V	
KMT RES	15K		H27E	-15V	
E34L RES	100Ω ½W & OHMS 10%		E34L	GND	
1 → PCI	100Ω ½W		D21S	D21C	

A-CP-KC09-C-27 External Components List for KC09-C (Sheet 1)

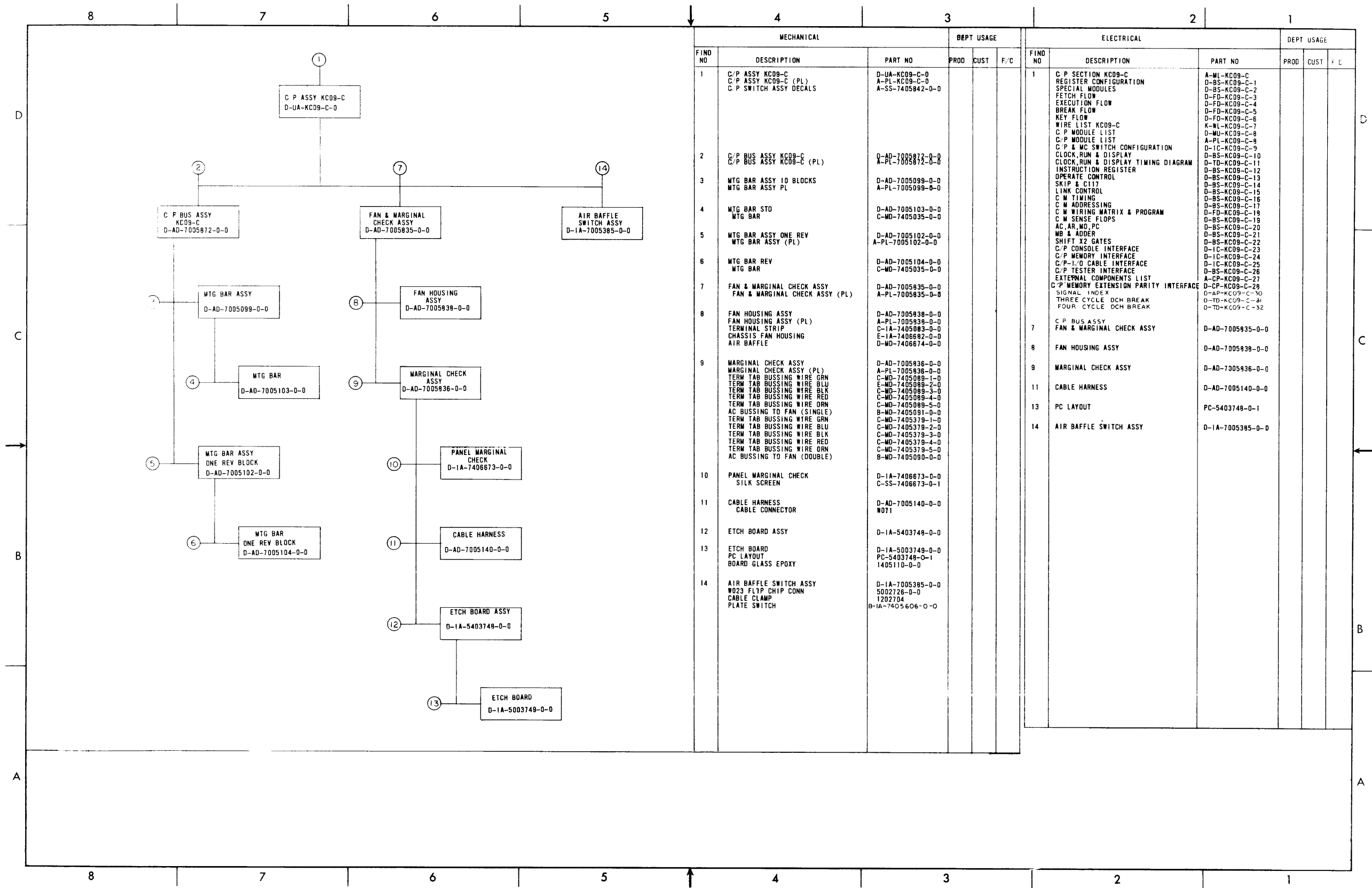
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COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
* JUMPER ADRL (B)	JUMPER		F02D	F03T	
* ACO → LINK	15K ½W		E04R	E04E	
SPEED WIPER	4700PF		J24T	J24C	
MEM STROBE	150Ω ½W		E31R	E31C	
**EXD (1) B	JUMPER		F37E	F36C	
**EPC03 (1)	JUMPER		F37K	F37C	
**EPC04 (1)	JUMPER		F37M	F38C	
E32N	100Ω ½W		D24H	D24C	
*F05T	JUMPER		F05T	F05C	
***API BK RQ	JUMPER		F22R	F22C	
EAE-P-PULSE	100Ω ½W		F02J	F02C	
E23N	100Ω ½W		C04J	C04C	
ACI	.001MFD & 150Ω		J12P	J12C	
*** JUMPERS REMOVED WHEN API IS INSTALLED					
** JUMPERS REMOVED WHEN KG09 MEM EXT CONTROL IS INSTALLED					
MEM STROBE	1K ½W		C01T	C01A	
MQI	.001MFD & 150Ω		C37T	C37C	

A-CP-KC09-C-27 External Components List for KC09-C (Sheet 2)



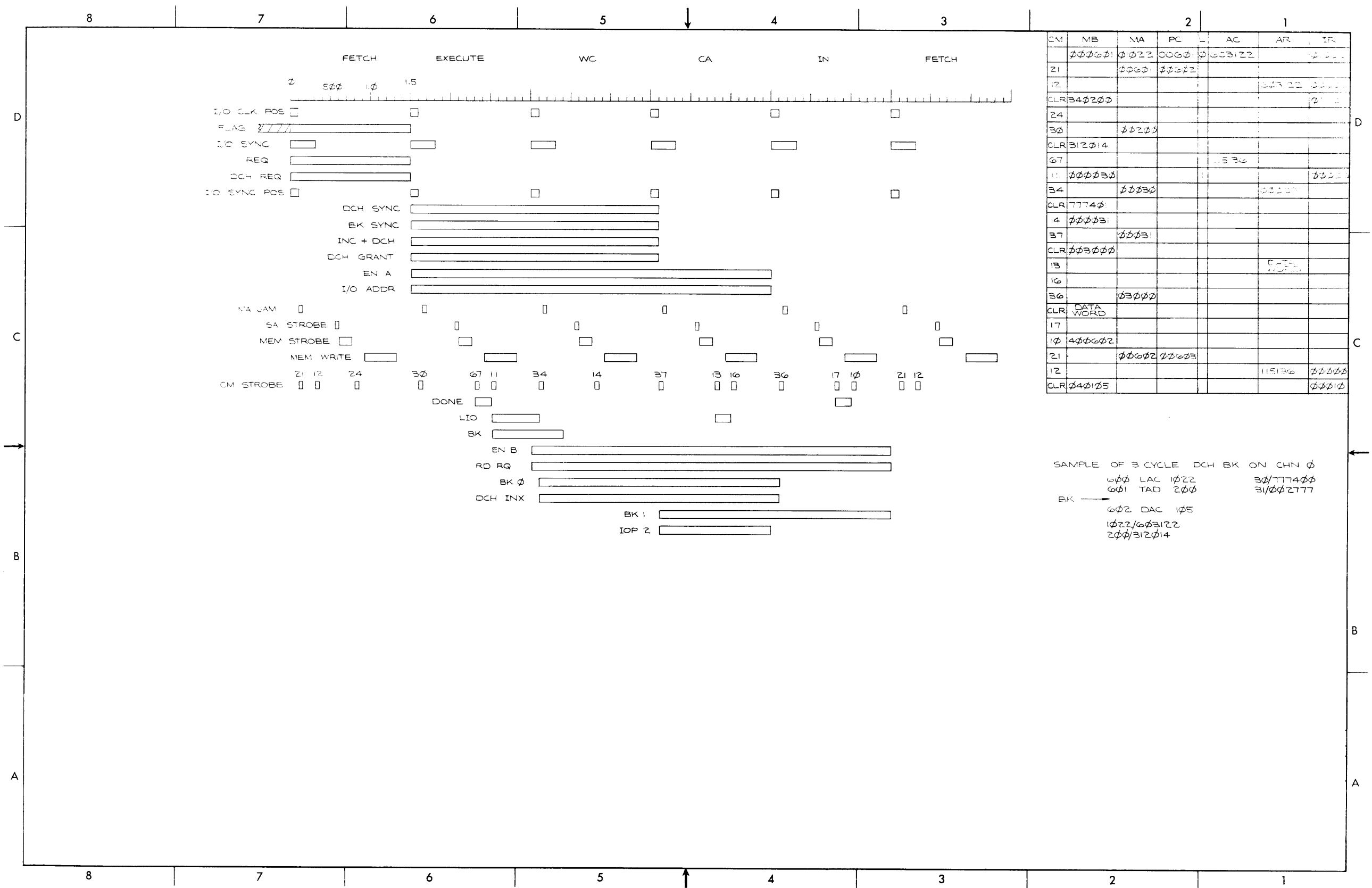
D-BS-KC09-C-28 CP - Memory Extended Parity Interface



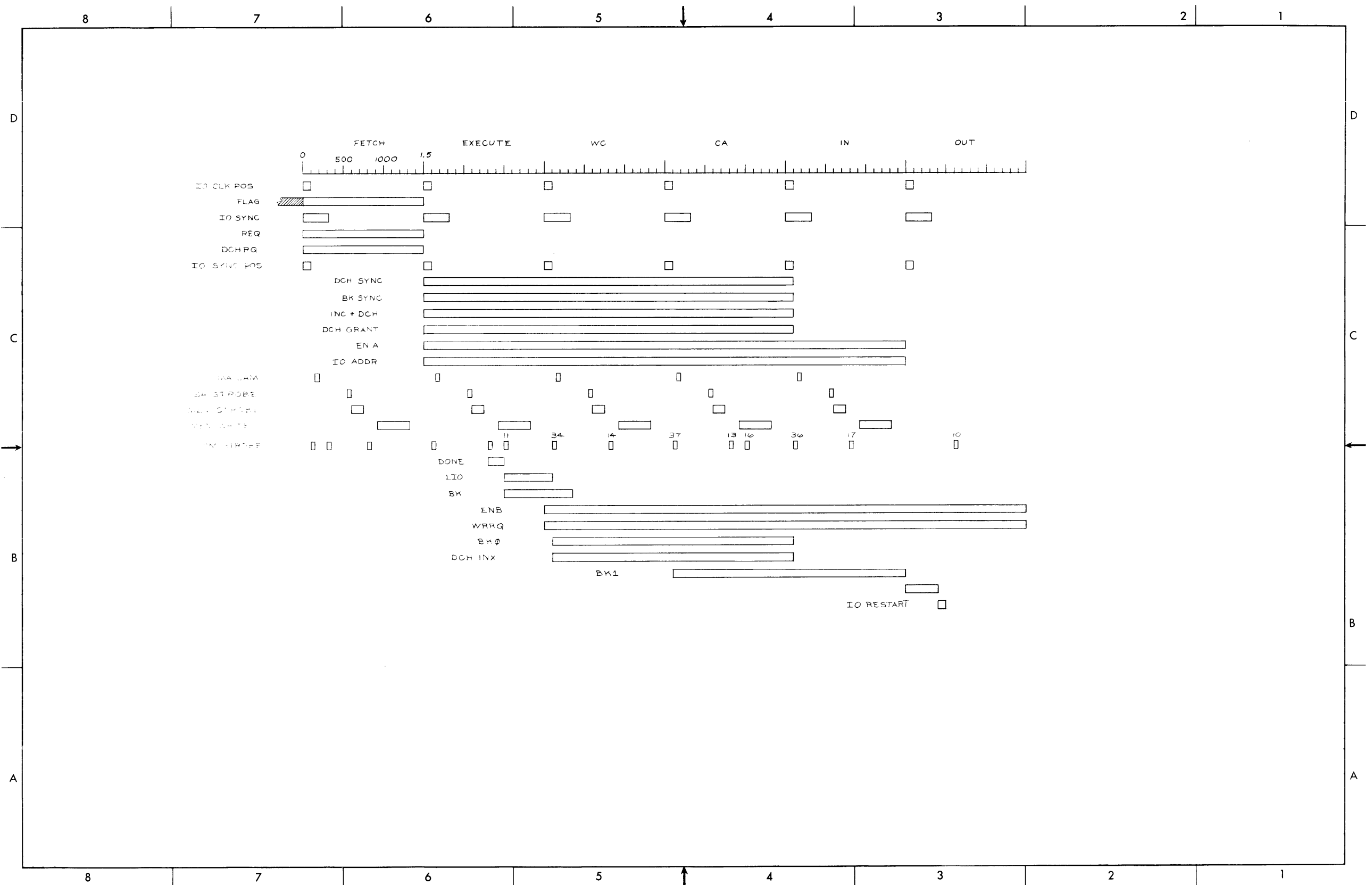
D-DI-KC09-C-29 Drawing Index List KC09-C

8			7			6			5			4			3			2			1					
SIGNAL NAME			ORIGIN			DESTINATION			SIGNAL NAME			ORIGIN			DESTINATION			SIGNAL NAME			ORIGIN			DESTINATION		
D	A	10				CMP (0-7)	17	21-1-2	KCT	9-0-3	10	.23(INTERFACE)	PKCLR	10	19-1, 12, 24(INTERF)	WR RQ		19-1-3, 10-								
	A BUS LINK	15, 3				CMP1	13	19-1-2-3	KCT(B)	10	.23(INTERFACE)	PROG SY(1)B	10	25(INTERF)			19-1									
	A BUS (00-05)	20-1				CMS1 (20-35)	17	3, 16	KDN	9-0-3	.23(INTERFACE)	PROG SYNC(1)B	12	25(INTERF)			19-1									
	A BUS (06-11)	20-2				CONT	19-1	15	KDP	10	.23(INTERFACE)	PWR OK	10	24(INTERF)			19-1									
	A BUS (12-17)	20-3				CO #1			KDP + KDN	10	.23(INTERFACE)															
	AC RD	INTERFACE-FROM 10	19-2, 25(INTERFACE)			CLR RQ	16		KDP + KON + RI	19-3	.25(INTERFACE)															
	AC SIGN	15							KDPM	9-0-5	23(INTERFACE), 10															
	AC 0 TO LINK	3							KEN	9-0-3	16, 15, 13, 17															
	AC (00-05)	20-1							KEY	19-2	25(INTERFACE)															
	AC (06-11)	20-2							KEY BUS	10																
	AC (12-17)	20-3							KEY BUS(B)	10																
	ACD	9-0-3	19-3, 23(INTERFACE)						KEY DLY	10	25(INTERFACE)															
	AC1	19-2	3, 20-1, 20-2, 20-3						KEY INIT POS	9-0-3	10	.23(INTERFACE)														
	ACD	19-3	3, 20-1, 20-2, 20-3						KEY(KDP + KON)	10	19-1, 26(INTERF), 16															
	AC RD (B)	19-2	13						KIO	9-0-3	19-3	.25&26(INTERF)														
	ADDR 10	17, 3							KIOA3	10																
	ADDF	15							KIOA4	10																
	ADR EQ 0 SAVE	15	14						KIOA5	10																
	ADR1 (B)	15	22, 3, 4						KMT	9-0-5	10	.23&25(INTERF)														
	ADR (00-05)	21-1	22, 20-1, 15						KRI	9-0-3	10	.23(INTERF)														
	ADR (06-11)	21-2	20-2, 22, 20-1						KSP	9-0-3	10	.23(INTERF)														
	ADR (12-17)	21-3	22, 20-2, 20-3						KST	9-0-3	10	.23(INTERF)														
	ADRA (0-1)	21-1, 21-2	14, 15						KXDM	9-0-3	25(INTERF), 10															
	ADRB (0-1)	21-2, 21-3	14, 15																							
	ADSD	19-2	13, 25(INTERFACE), 16																							
	AM SYNC BUS(0)	19-1	21-1-2-3, 13																							
	AND	9-0-3	17, 25(INTERFACE)																							
	API BK RD, 1-B	9-0-3	23, 25(INTERFACE)																							
	API D	9-0-3	23(INTERF), 19-3																							
	AR (00-05)	20-1																								
	AR (06-11)	20-2																								
	AR (12-17)	20-3																								
	ARI	19-2	20-1-2-3, 15, 13, 10																							
	ARD	19-3	10																							
	ARD RESTORE	10																								
	ARDS	14																								
	AUT INX	14																								
	AXS	19-2	14, 13, 15																							
	C	AR	10																							
		AR (00-05)	20-1																							
AR (06-11)		20-2																								
AR (12-17)		20-3																								
ARD		19-2																								
ARD RESTORE		10																								
ARDS		14																								
AUT INX		14																								
AXS		19-2	14, 13, 15																							
AR		10																								
B	B BUS (00-05)	71-1																								
	B BUS (06-11)	71-2																								
	B BUS (12-17)	21-3																								
	BK SYNC																									
	BK D(0)B																									
	BK D(1)B																									
	BK D(2)B																									
	BK D(3)B																									
	BK D(4)B																									
	BK D(5)B																									
A	CAL	12																								
	CI 17	3, 14																								
	CJIT	19-2																								
	CLK	10																								
	CLK D	10																								
	CLK (B)	10																								
	CLK EN	10																								
	CLK POS	10																								
	CLK+RUN	10																								
	CLL	13																								
CLR	16																									
LLR1	19-2																									
CW CLK	10																									
CW CURRENT	16																									
CW STROBE A	16																									
CW STROBE B	16																									
CW STROBE C	16																									
CW STROBE D	16																									
CW STROBE DLYD	16																									
CWA (00-05)	19-1																									
CWG (0-7)	17																									
CWL	13																									

D-AP-KC09-C-30 Signal Index



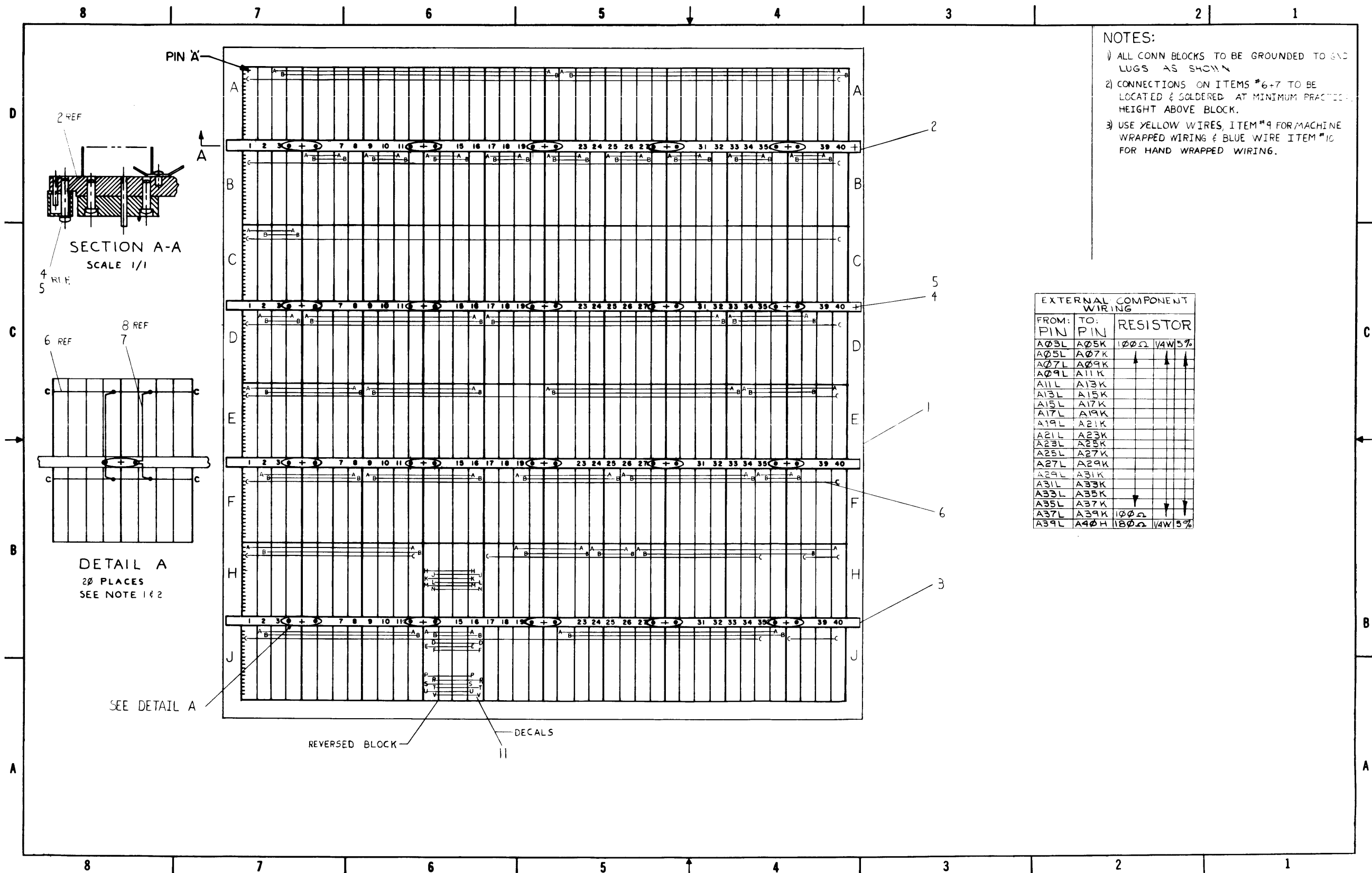
D-TD-KC09-C-31 Three Cycle DCH Break



D-TD-KC09-C-32 Four Cycle DCH Break

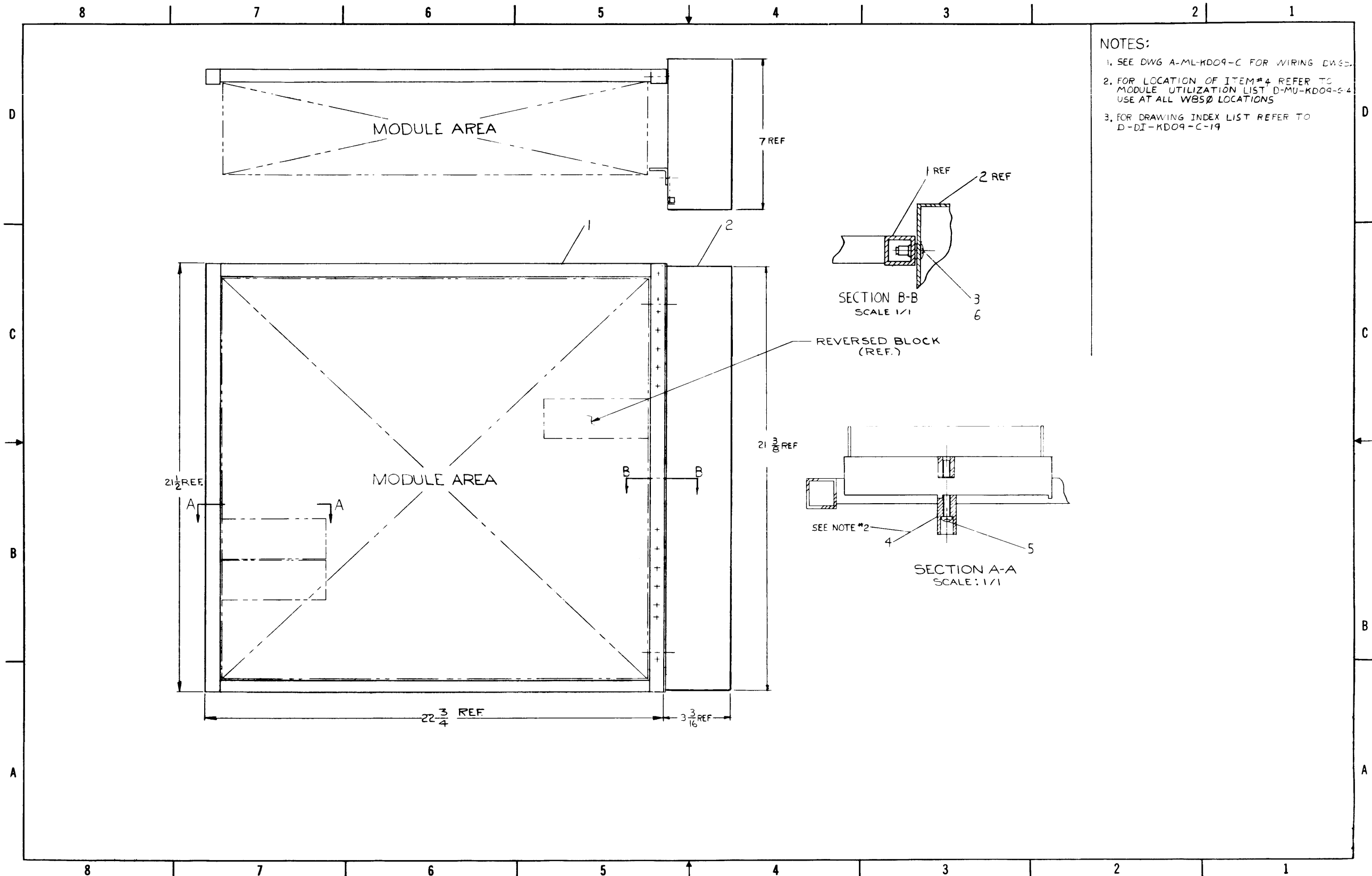
DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS PARTS LIST			QUANTITY/VARIATION																	
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION																		
1	E-IA-7405034-0-0	DOOR FRAME	1																	
2	D-AD-7005099-0-0	MTG BAR ASSY (CONN. BLOCKS)	3																	
3	D-AD-7005102-0-0	MTG BAR ASSY (ONE REVERSE BLOCK)	1																	
4	9006043-1	SCREW PHIL PAN HD #8-32 x 1 SST	8																	
5	9006634	WASHER LOCK INT TOOTH # SST	8																	
6	1202188	VOLTAGE CHAIN	A/R																	
7	9107560-1	#22 AWG SOLID WIRE	A/R																	
8	9107265	#22 AWG SLEEVING (WHT)	A/R																	
9	9107470-5	#24 AWG SOLID KYNAR YEL	A/R																	
10	9107470-10	#24 AWG SOLID KYNAR BLU	A/R																	
11	A-DC-7406747-0-0	DECALS, REVERSED BLOCK	A/R																	
	KC09-C-7	WIRE LIST KC09-C	REF.																	
	KC09-C-27	EXTERNAL COMPONENTS LIST	REF.																	

A-PL-7005872-0-0 Central Processor Bus Assembly

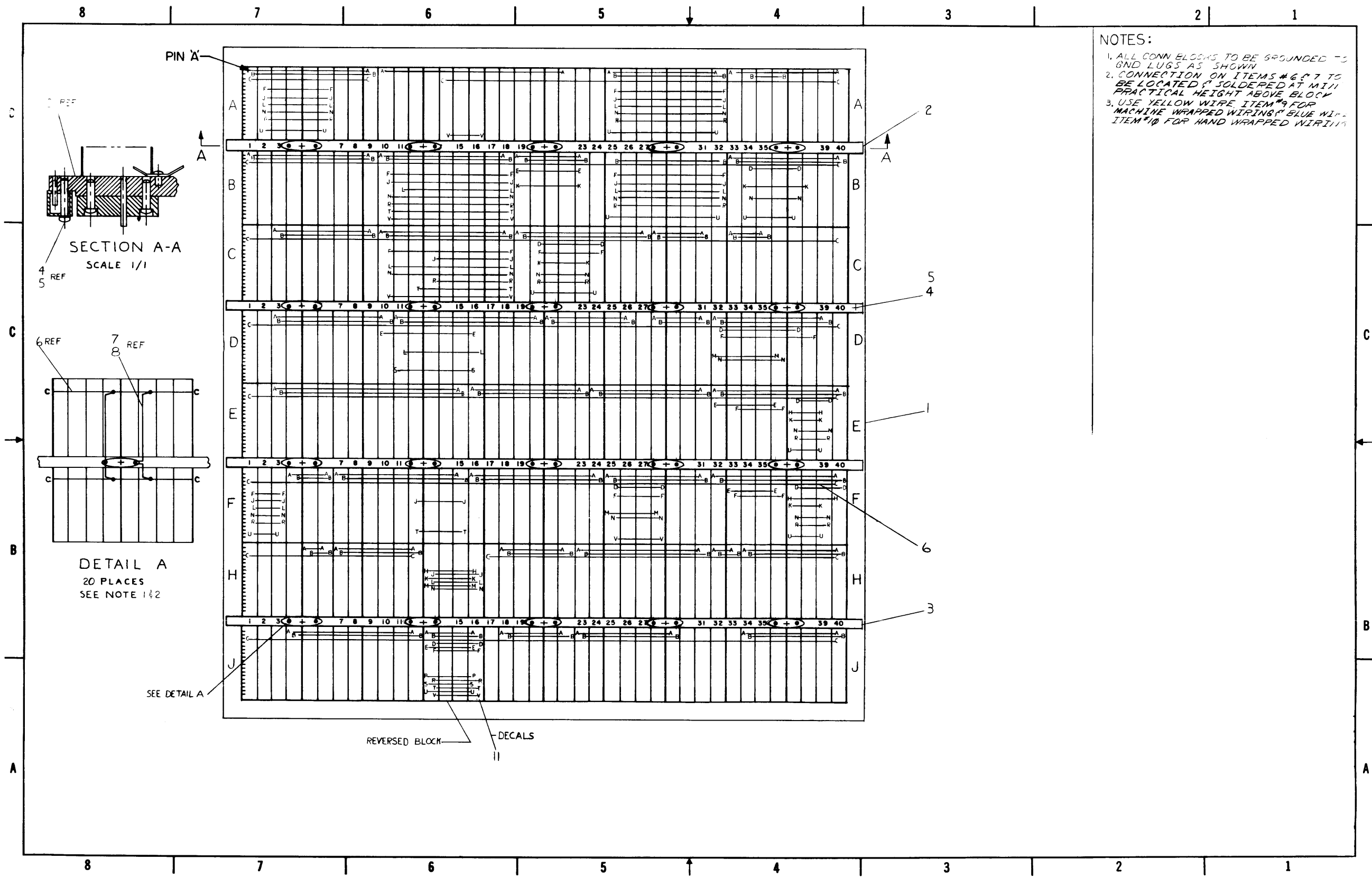


NOTES:

- 1) ALL CONN BLOCKS TO BE GROUNDED TO GND LUGS AS SHOWN
- 2) CONNECTIONS ON ITEMS #6-7 TO BE LOCATED & SOLDERED AT MINIMUM PRACTICAL HEIGHT ABOVE BLOCK.
- 3) USE YELLOW WIRES, ITEM #9 FOR MACHINE WRAPPED WIRING & BLUE WIRE ITEM #10 FOR HAND WRAPPED WIRING.



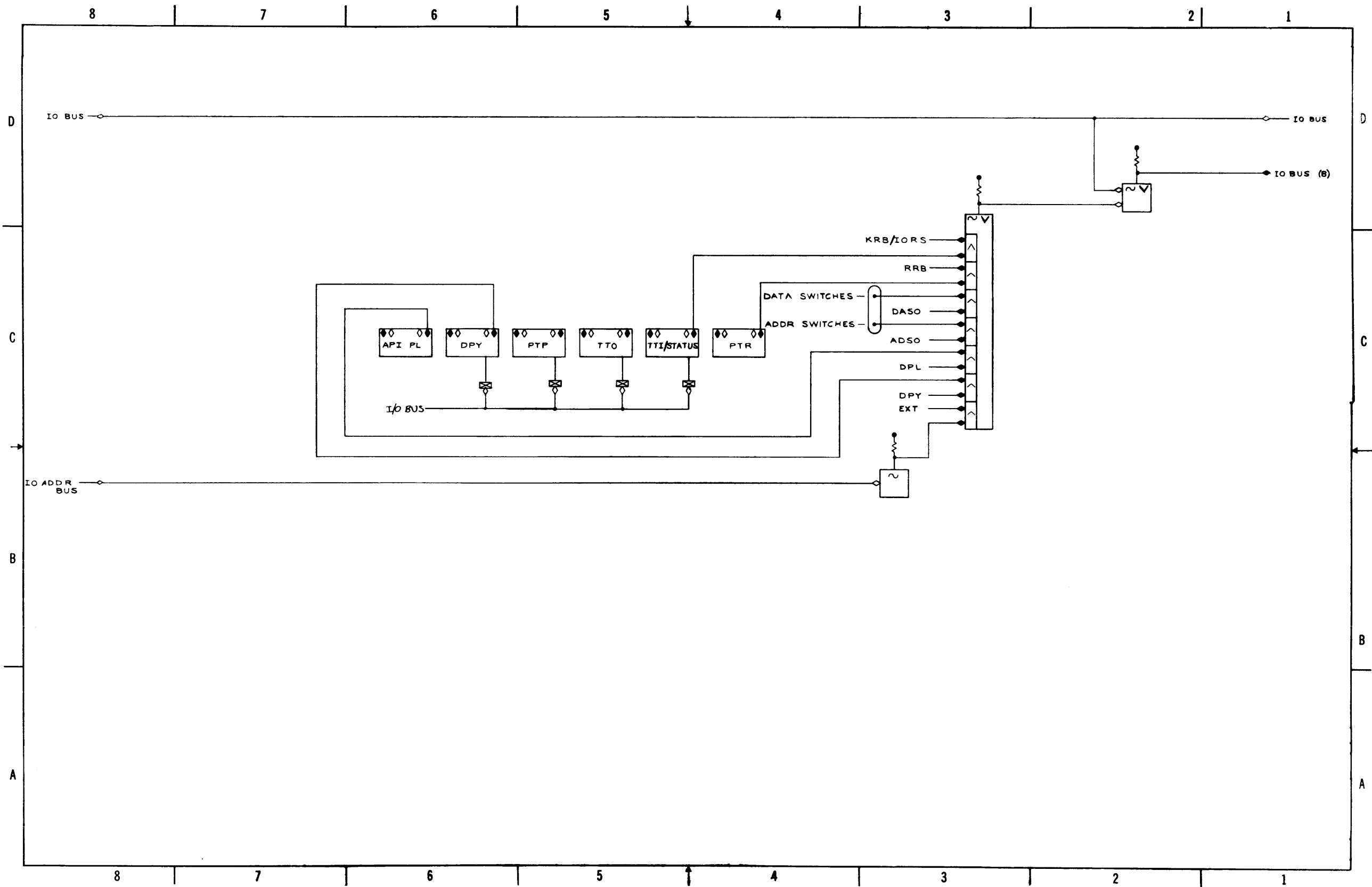
D-UA-KD09-C-0 I/O Assembly KD09-C



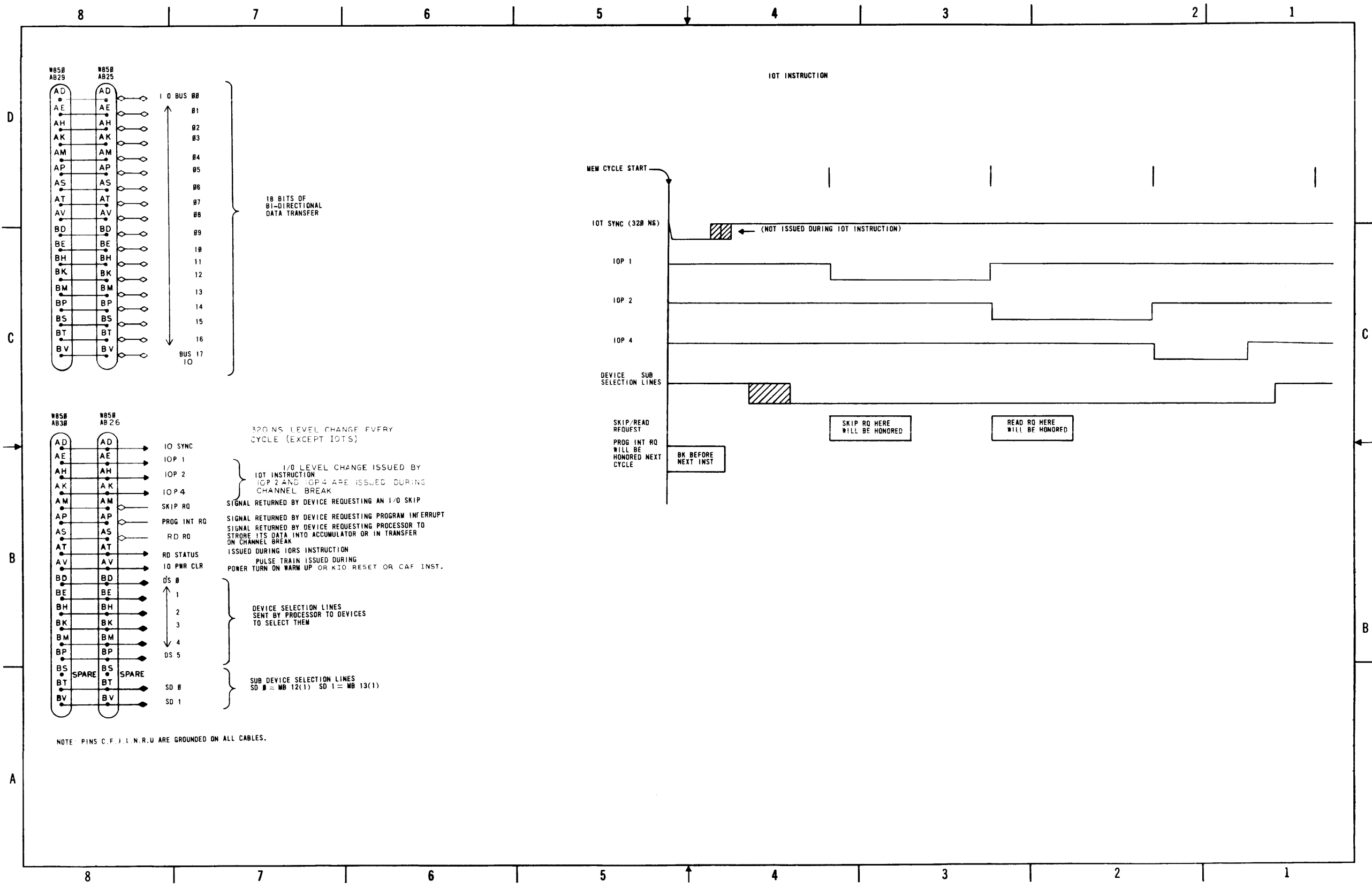
- NOTES:
1. ALL CONN BLOCKS TO BE GROUNDED TO GND LUGS AS SHOWN
 2. CONNECTION ON ITEMS #6 & 7 TO BE LOCATED & SOLDERED AT MIN PRACTICAL HEIGHT ABOVE BLOCK
 3. USE YELLOW WIRE ITEM #9 FOR MACHINE WRAPPED WIRING & BLUE WIRE ITEM #10 FOR HAND WRAPPED WIRING

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS PARTS LIST			QUANTITY / VARIATION															
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION																
1	E-IA-7405034-0-0	DOOR FRAME	1															
2	D-AD-7005099-0-0	MTG BAR ASSY (CONN.BLOCK)	3															
3	D-AD-7005102-0-0	MTG BAR ASSY (ONE REVERSE BLOCK)	1															
4	9006043-1	SCREW PHIL PAN HD #8-32 x 1 SST	8															
5	9006634	WASHER LOCK INT TOOTH # SST	8															
6	1202188	VOLTAGE CHAIN	A/R															
7	9107560-1	#22 AWG SOLID WIRE	A/R															
8	9107265	#22 AWG SLEEVING (WHT)	A/R															
9	9107470-5	#24 AWG SOLID KYNAR YEL	A/R															
10	9107470-10	#24 AWG SOLID KYNAR BLU	A/R															
11	A-DC-7406747-0-0	DECALS, REVERSED BLOCK	A/R															
	K-WL-KD09-C-15	WIRE LIST KD09-C	REF															
	A-CP-KD09-C-16	EXTERNAL COMPONENTS LIST	REF															

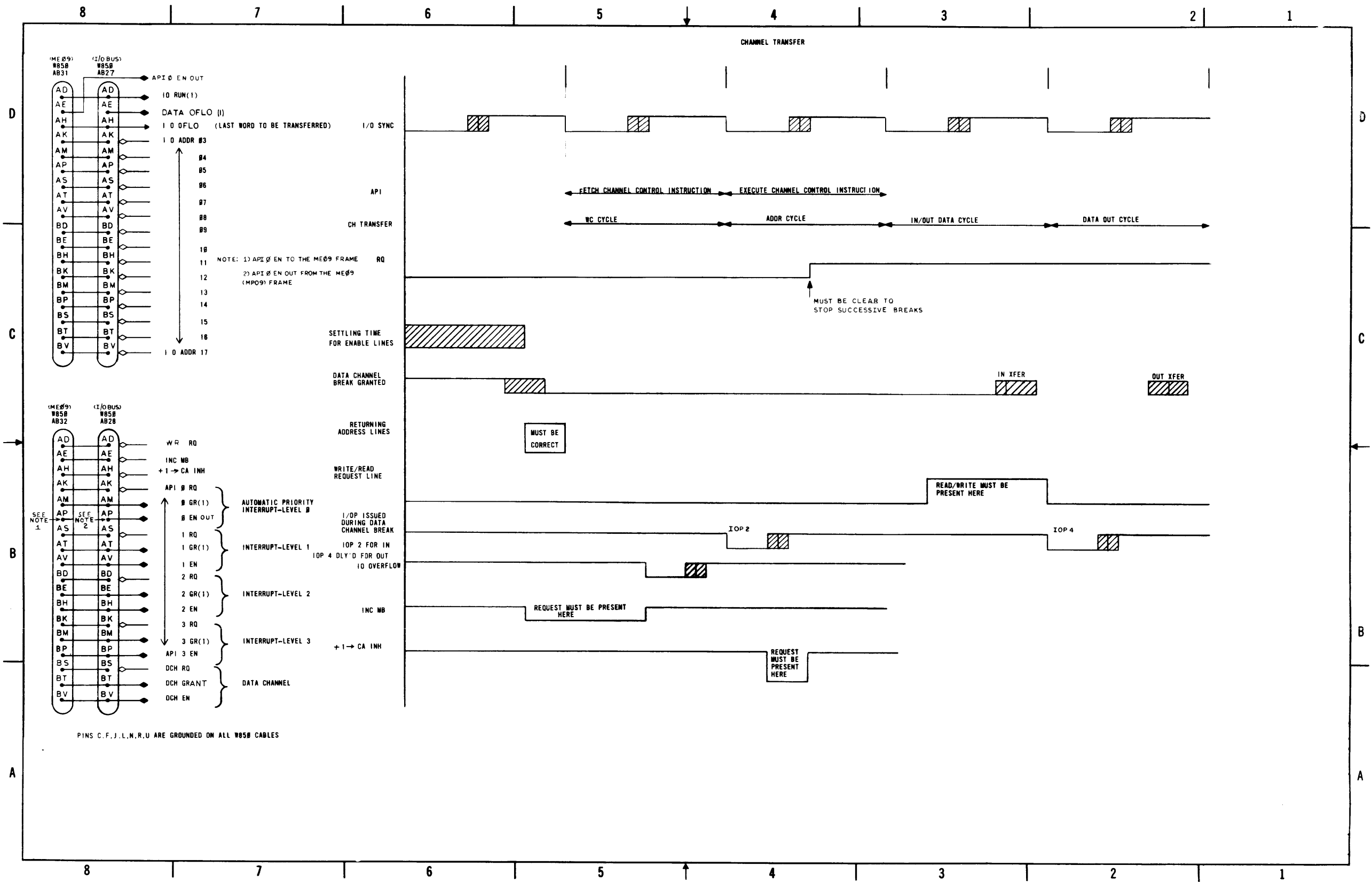
A-PL-7005873-0-0 I/O Bus Assembly KD09



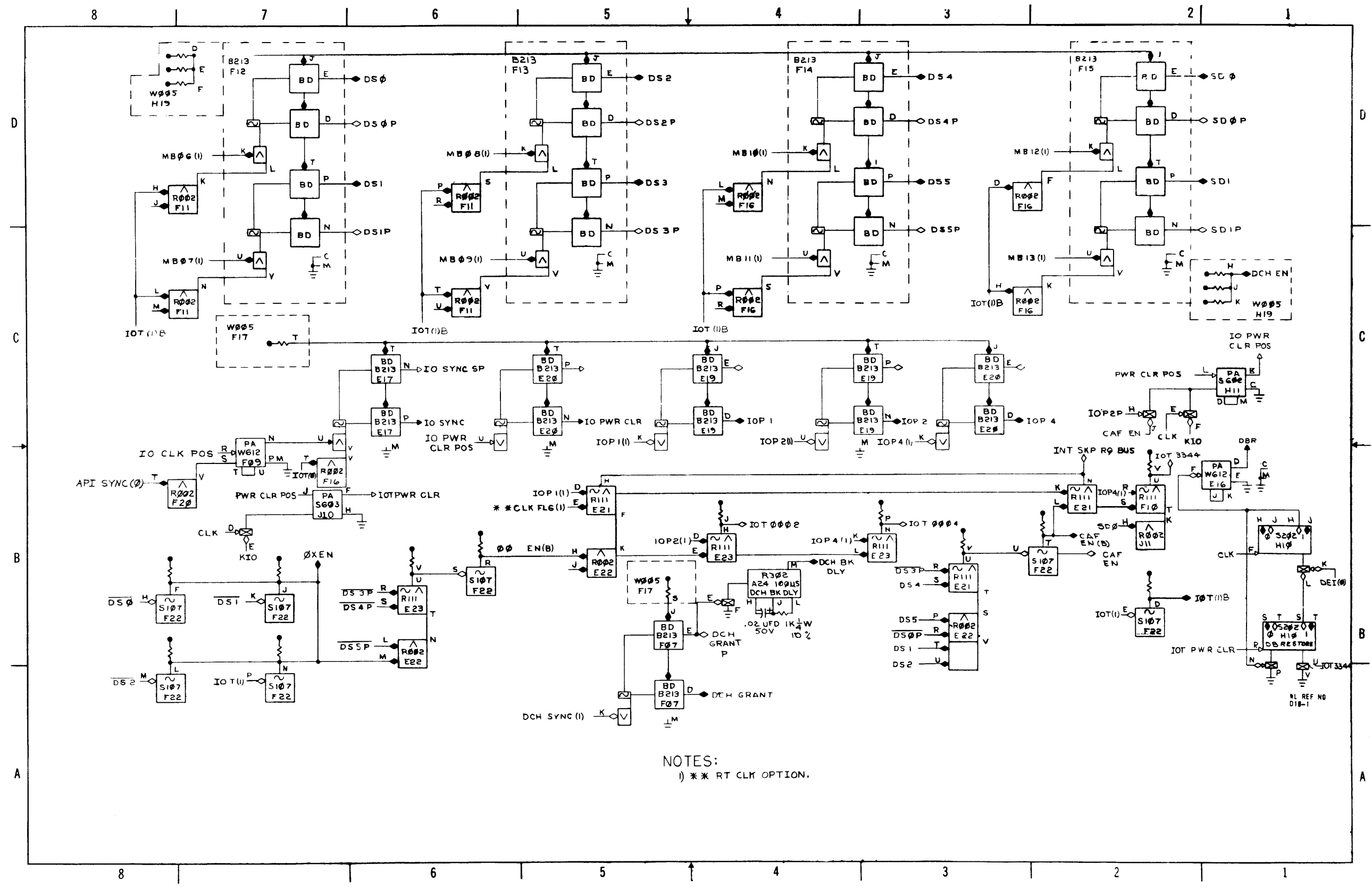
D-BS-KD09-C-1 IO Configuration



D-TD-KD09-C-2 IO Bus Interface (Sheet 1)

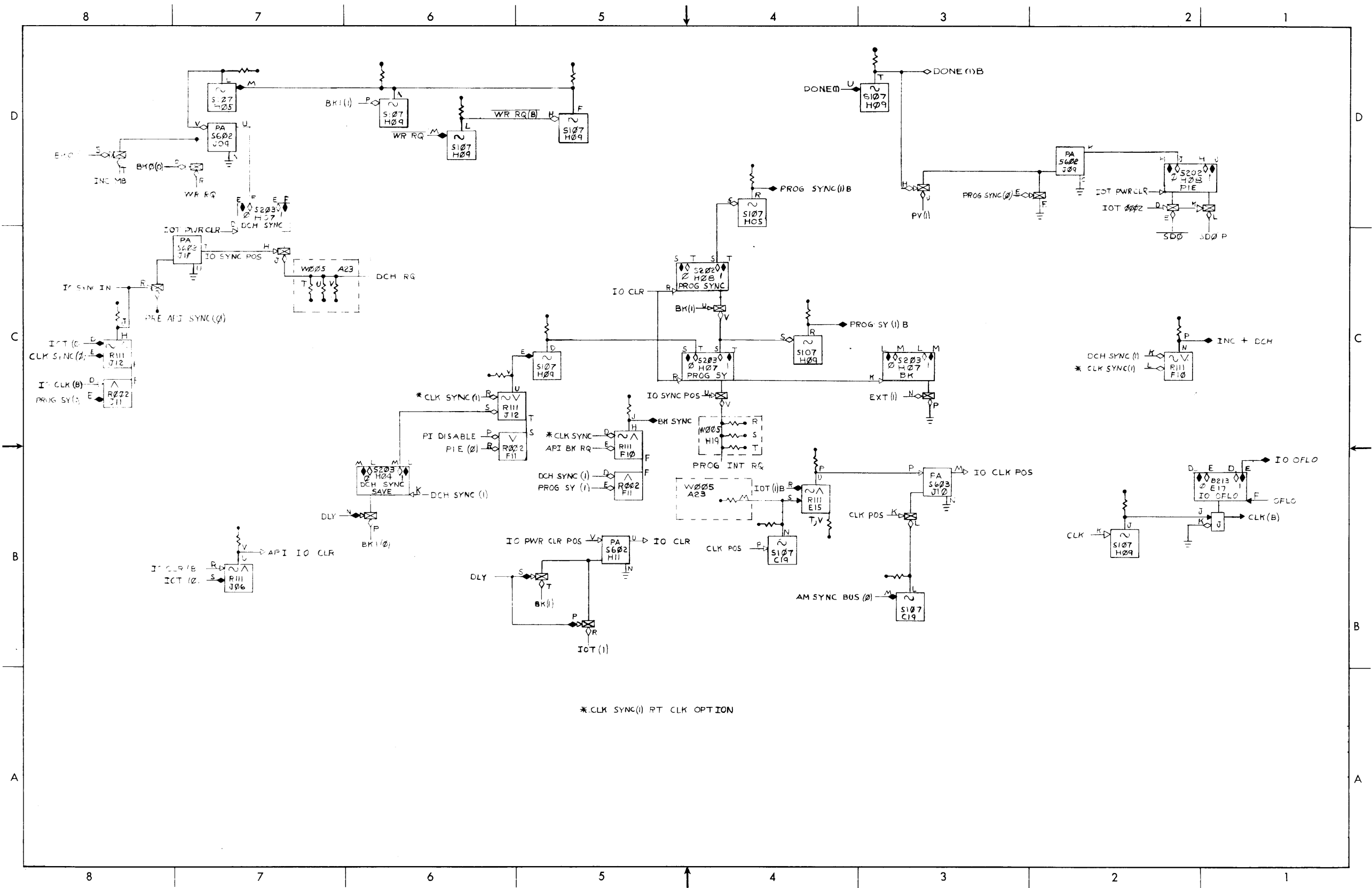


D-TD-KD09-C-2 IO Bus Interface (Sheet 2)

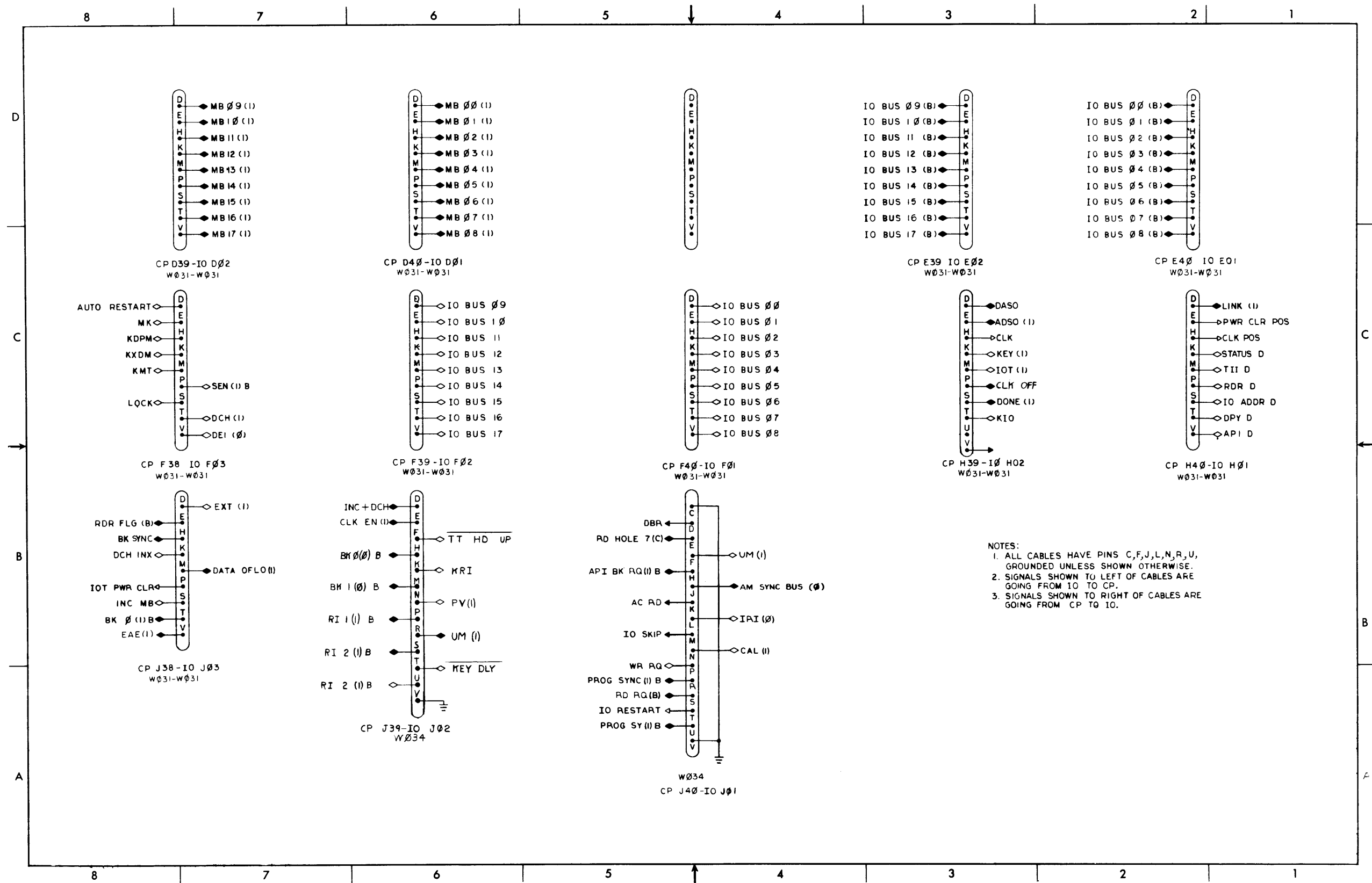


NOTES:
) ** RT CLK OPTION.

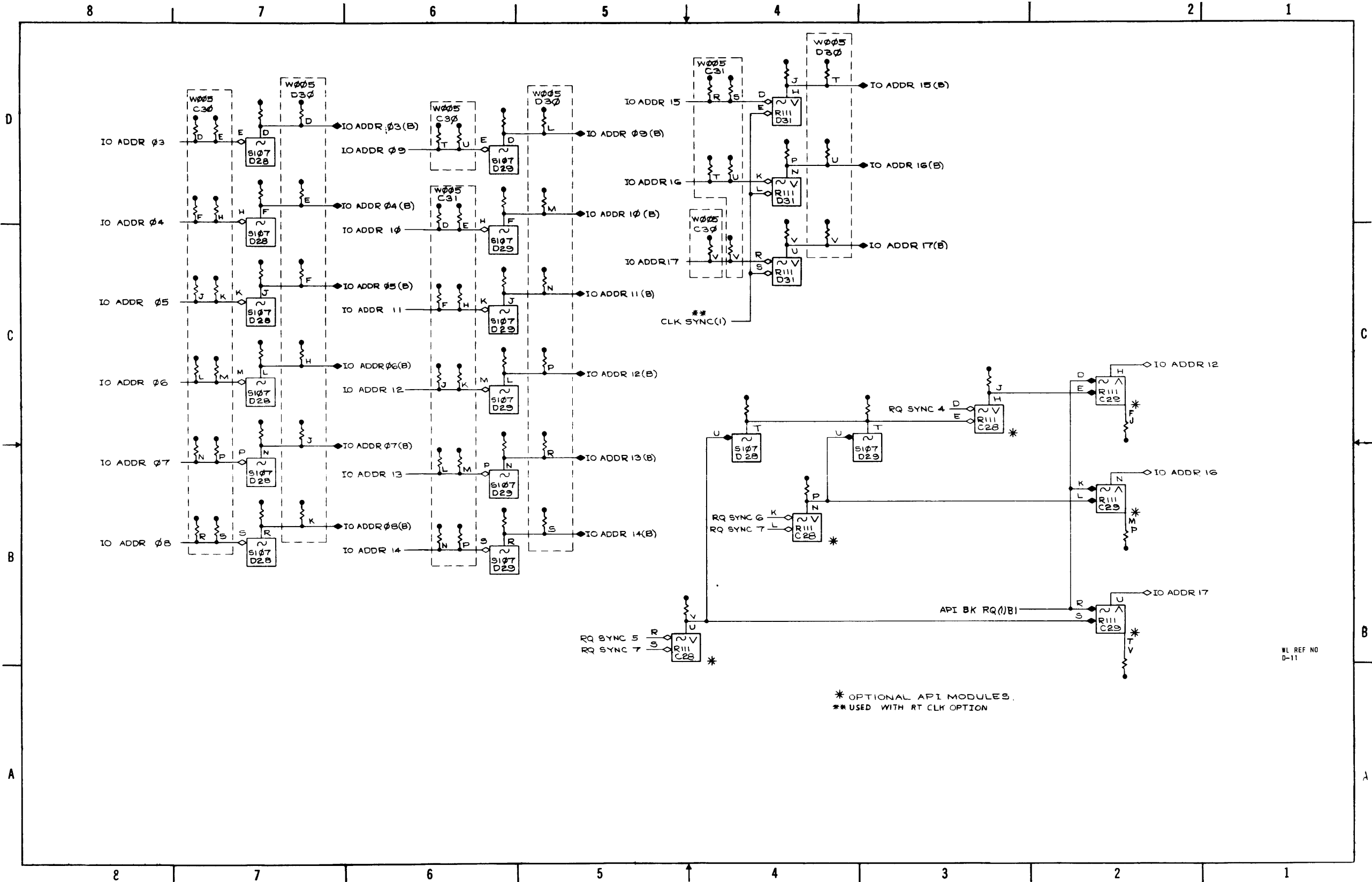
D-B5-KD09-C-3 IO Control (Sheet 1)



D-BS-KD09-C-3 IO Control (Sheet 2)



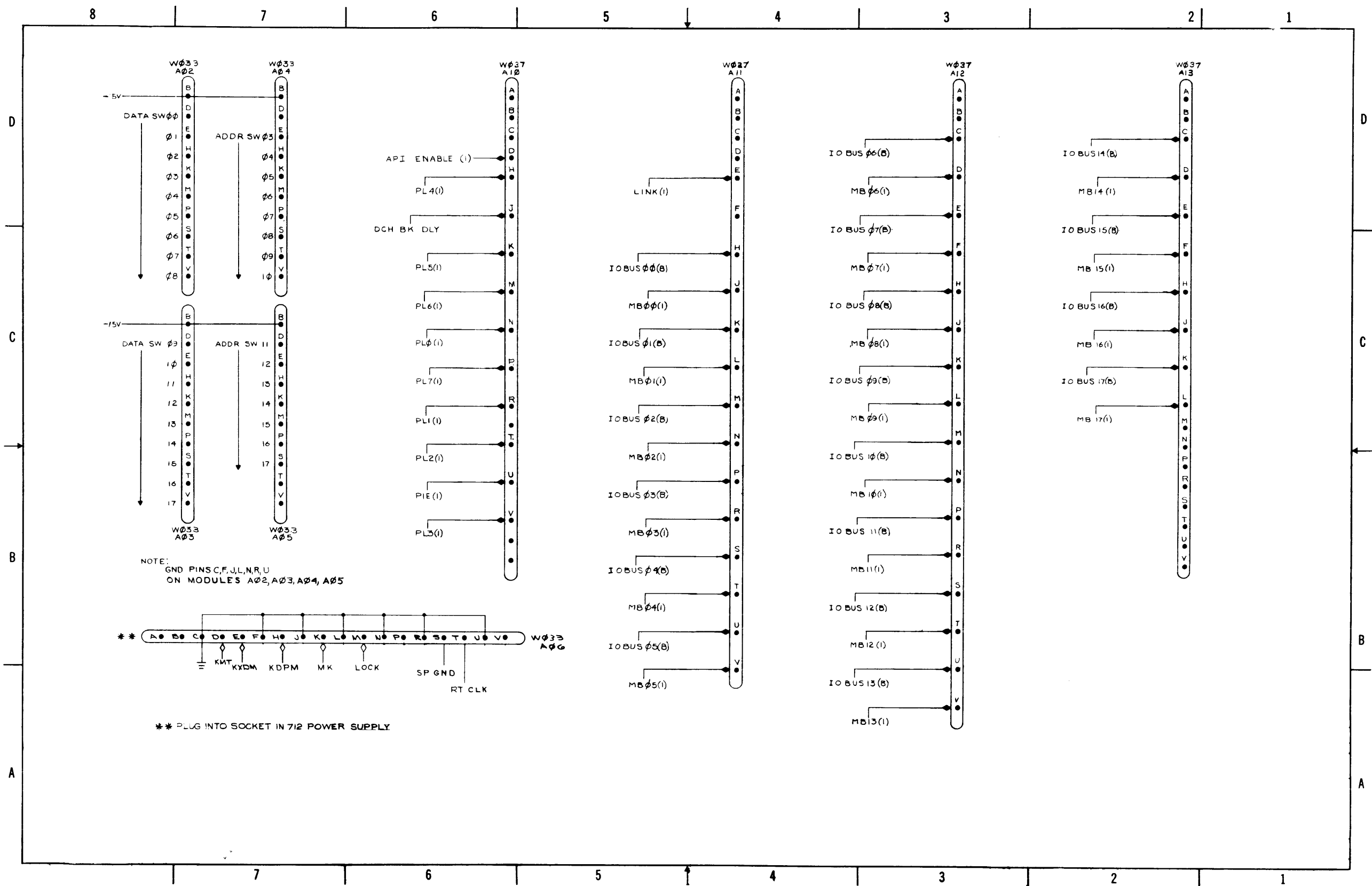
D-IC-KD09-C-4 CP - IO Cable Interface



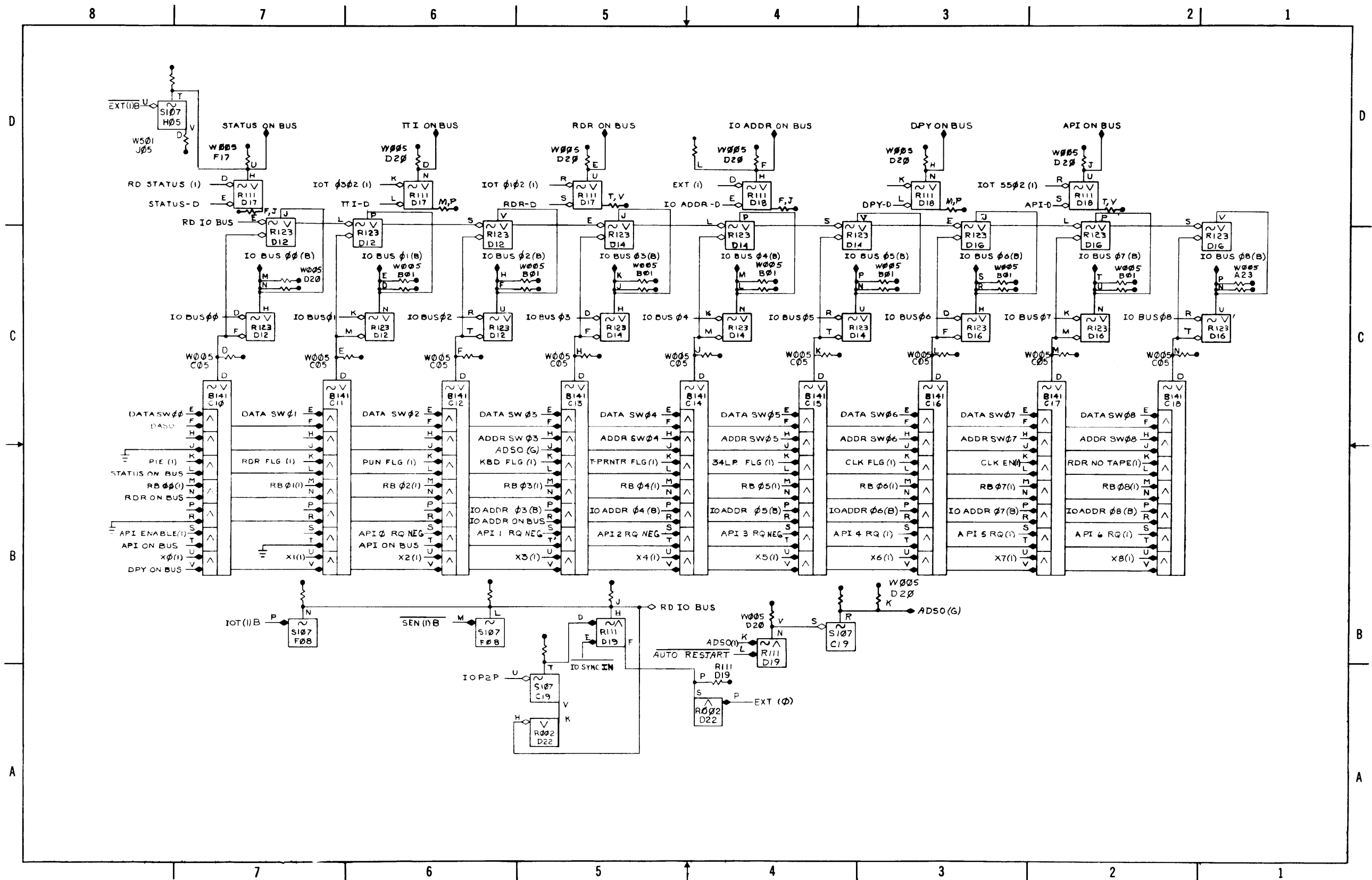
D-BS-KD09-C-5 ADDR Bus

* OPTIONAL API MODULES.
 ** USED WITH RT CLK OPTION

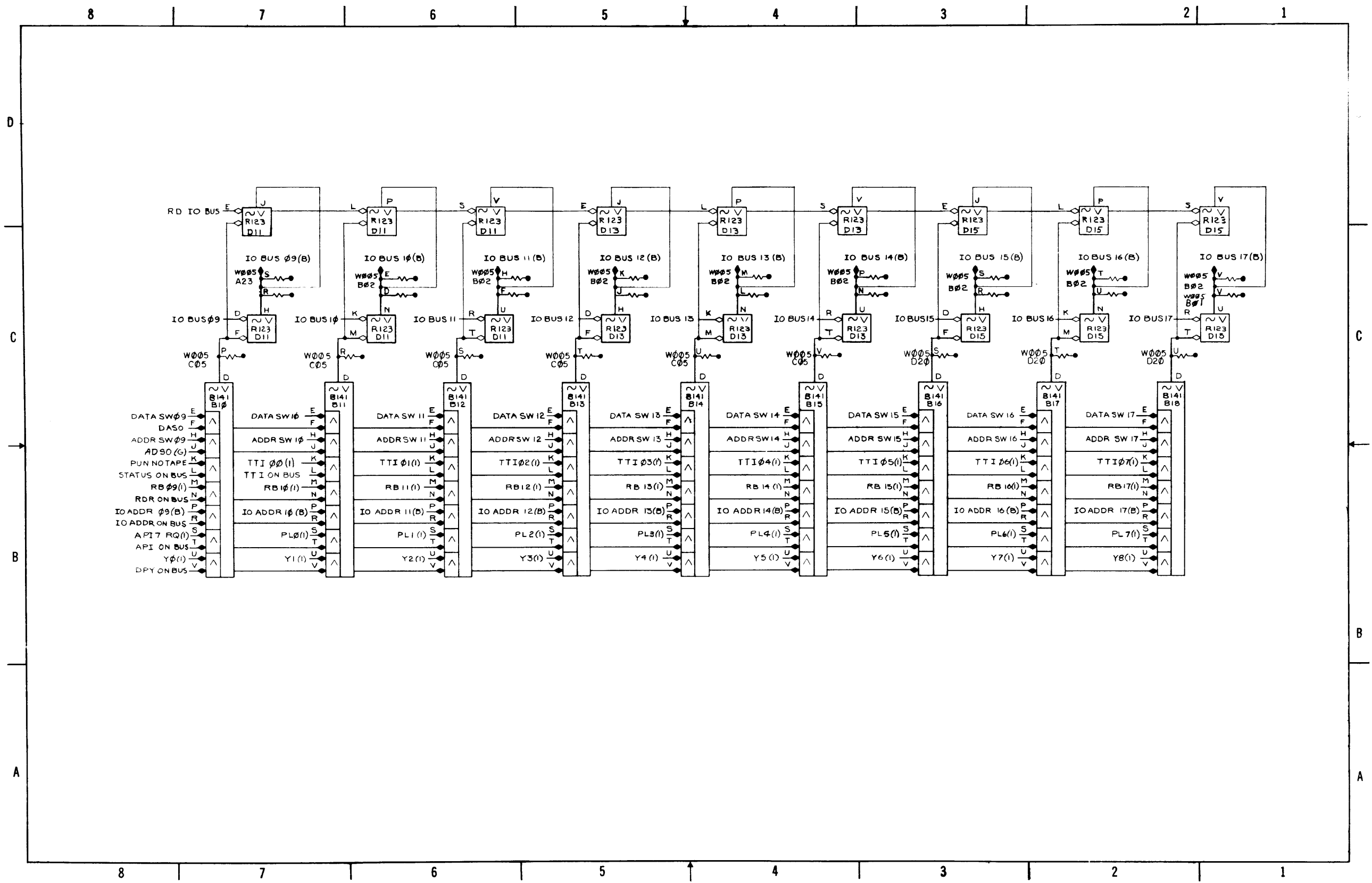
WL REF NO
 D-11



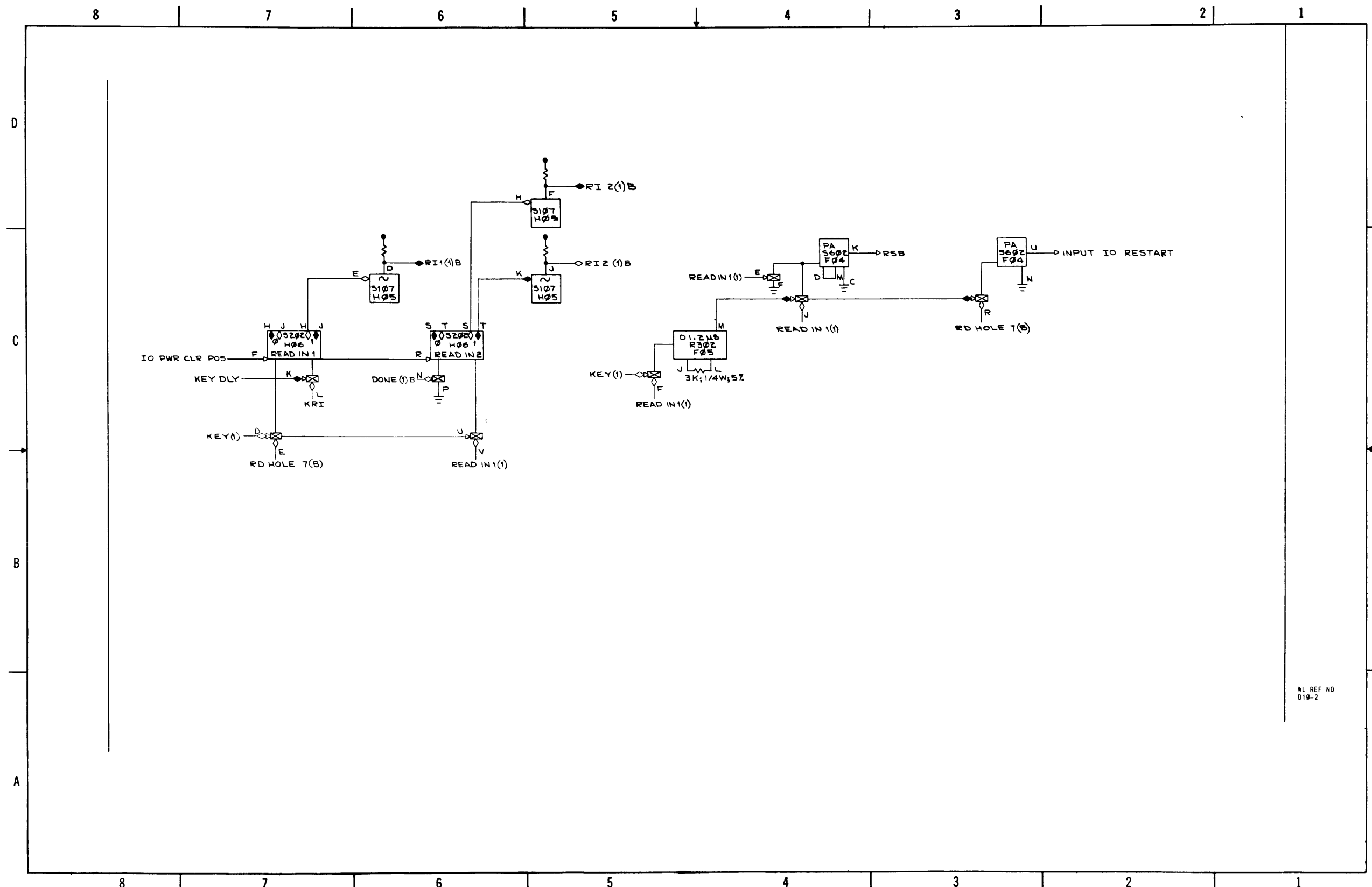
D-BS-KD09-C-6 IO/Console Interface



D-BS-KD09-C-7 Input Mixer (Sheet 1)

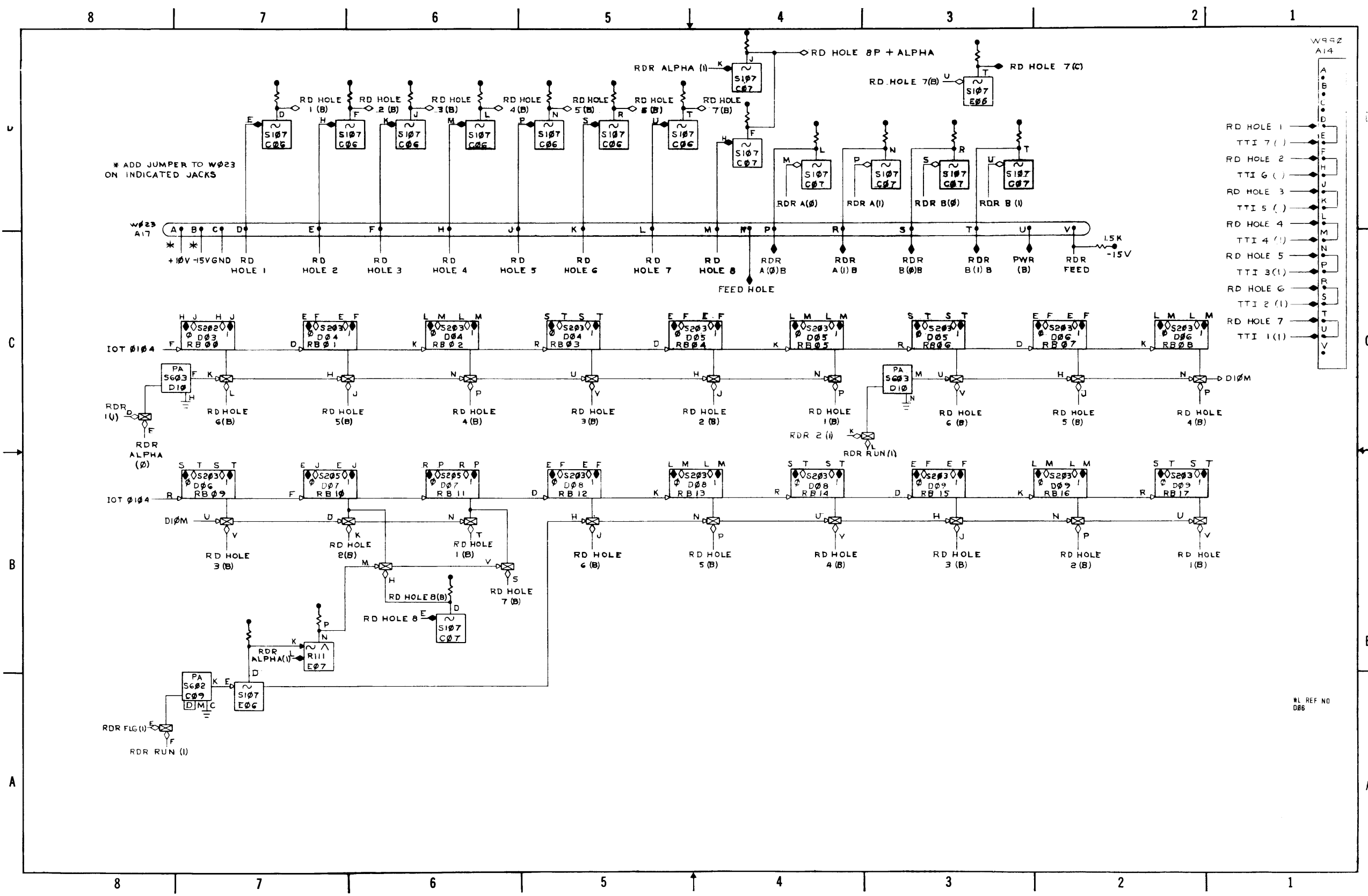


D-BS-KD09-C-7 Input Mixer (Sheet 2)

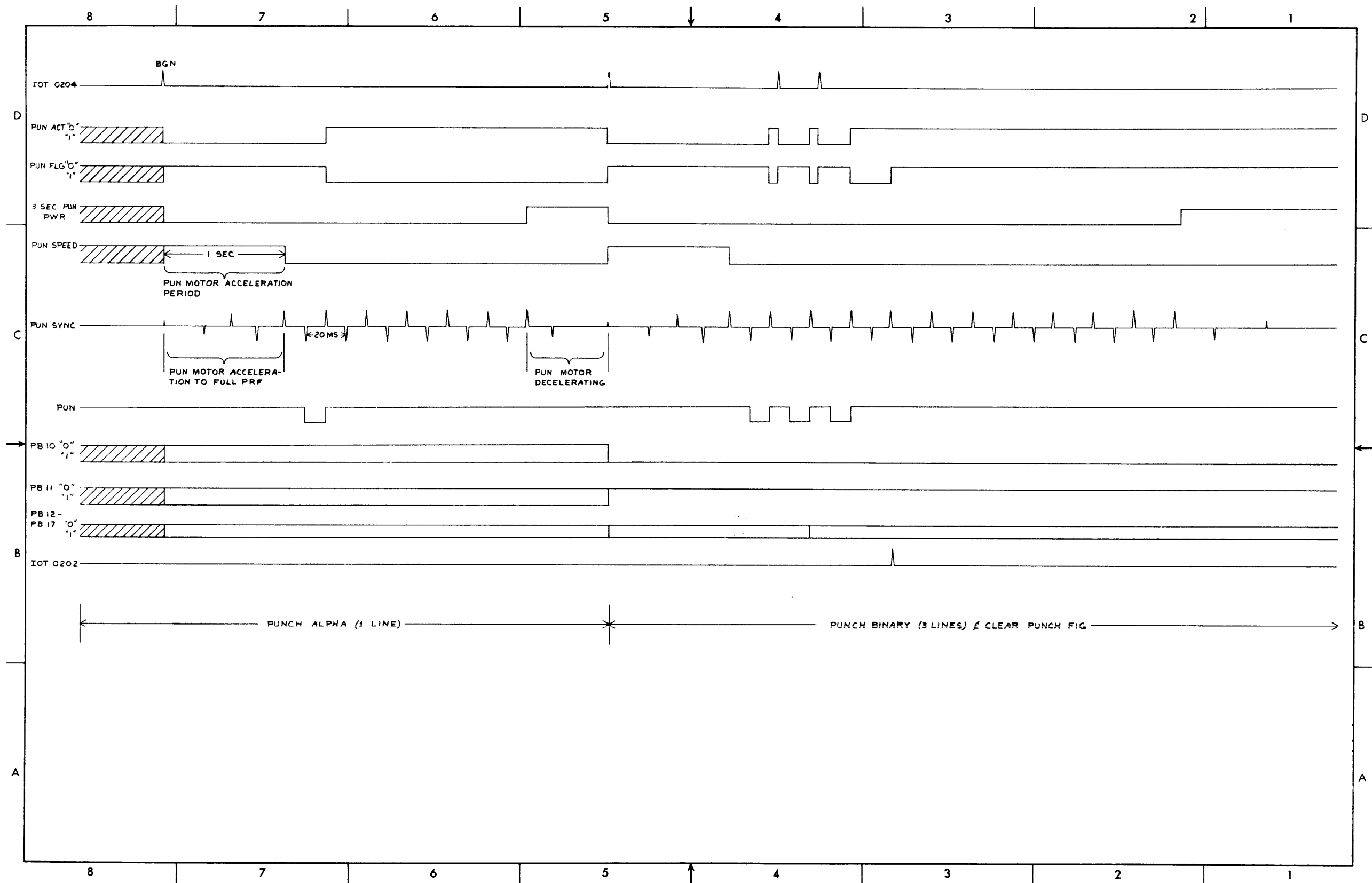


NL REF NO
D10-2

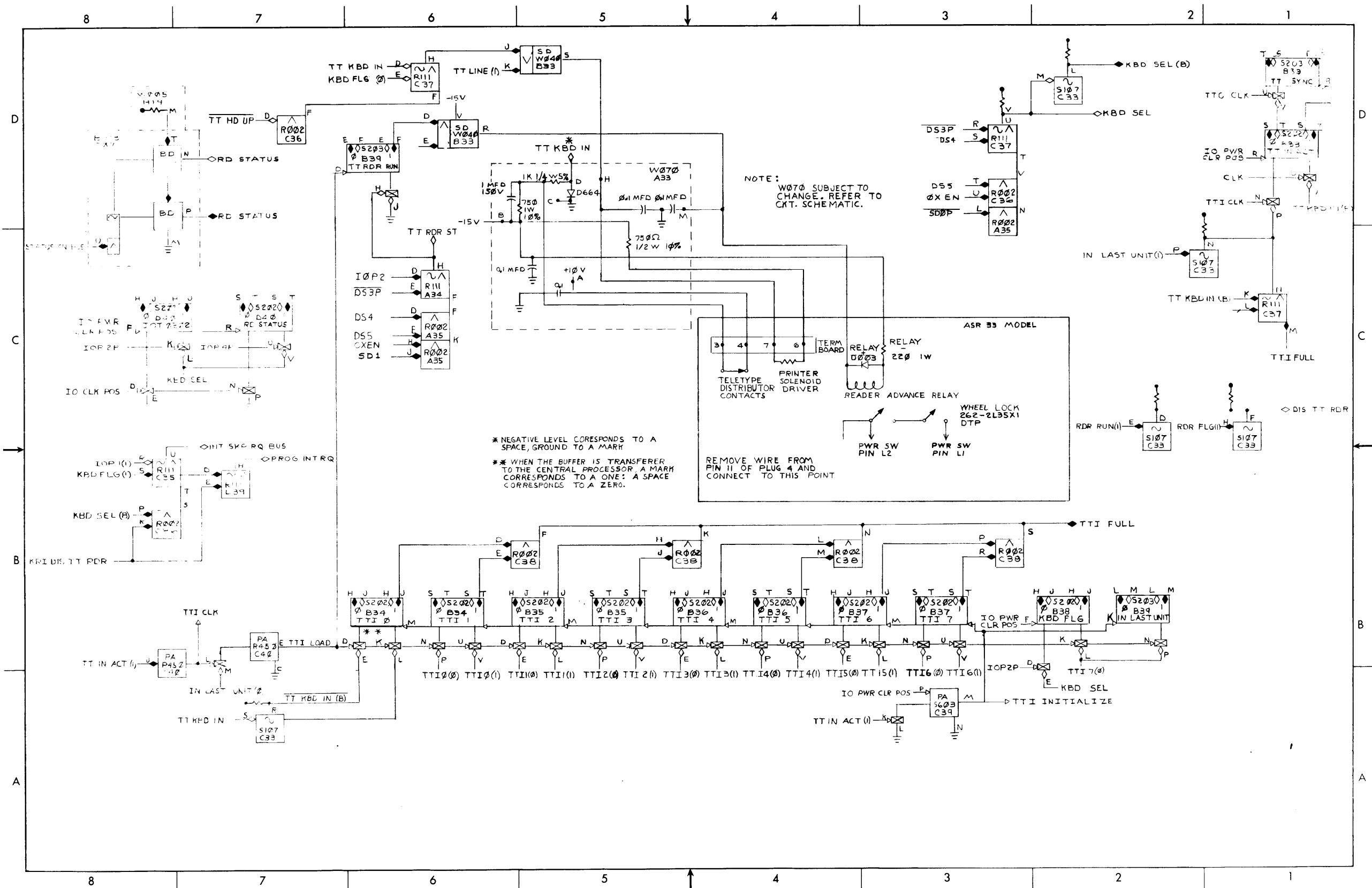
D-BS-KD09-C-8 Read In Mode



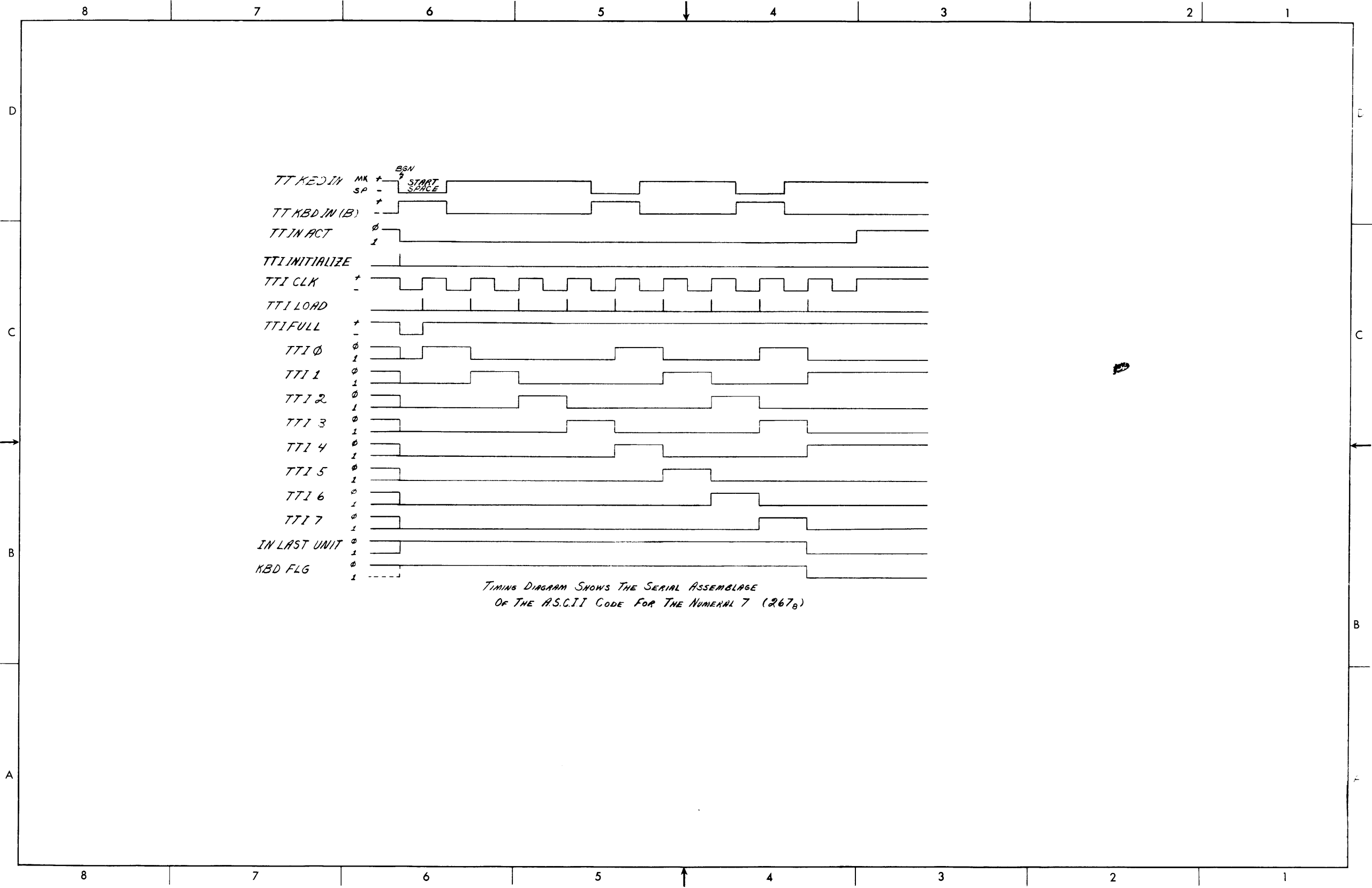
D-BS-KD09-C-9 Reader Control (Sheet 2)



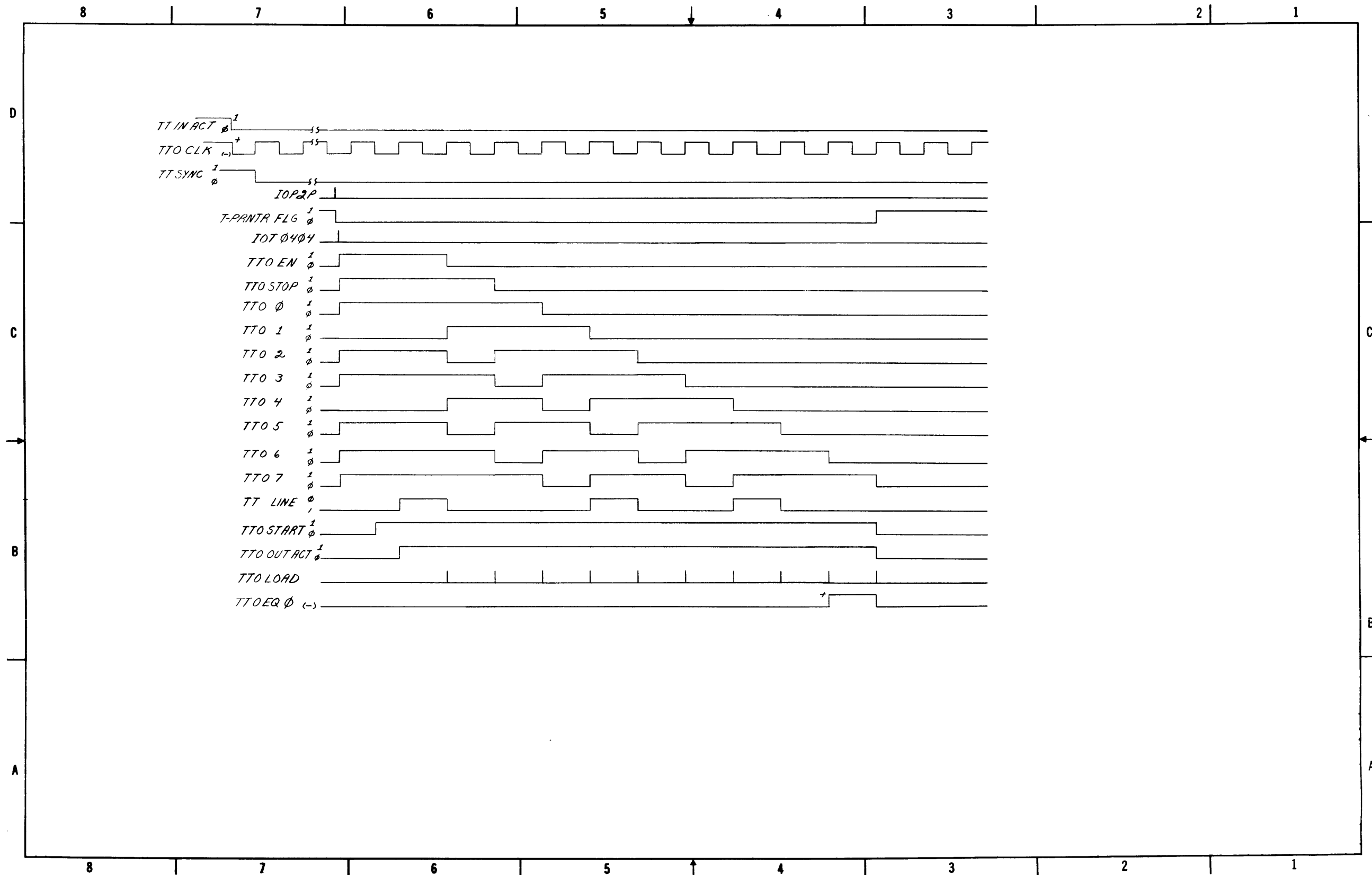
D-TD-KD09-C-10 Punch Control Timing Diagram



D-BS-KD09-C-11 Teletype Control (Sheet 1)



TIMING DIAGRAM SHOWS THE SERIAL ASSEMBLY OF THE ASCII CODE FOR THE NUMERAL 7 (267₈)



D-TD-KD09-C-12 Teletype Control Time (Keyboard) (Sheet 2)

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS PARTS LIST			QUANTITY / VARIATION									
ITEM NO.	DWG NO. / PART NO.	DESCRIPTION										
	S603	PULSE AMPLIFIER	5									
	S602	PULSE AMPLIFIER	6									
	S202	DUAL FLIP FLOP	16									
	S203	TRIPLE FLIP FLOP	9									
	S205	DUAL FLIP FLOP	7									
	S107	INVERTER	13									
	R002	DIODE NETWORK	11									
	R111	EXPANDABLE NAND/NOR GATE	22									
	R123	INPUT BUS	6									
	R302	DELAY (ONE SHOT)	3									
	R450	VARIABLE CLOCK	1									
	R141	AND/NOR GATE	1									
	B141	DIODE GATE	18									
	B213	JAM FLIP FLOP	8									
	B301	DELAY	2									
	W005	CLAMPED LOAD	11									
	W040	SOLENOID DRIVER	1									
	W612	PULSE AMPLIFIER	3									
	W990	BLANK MODULE	2									
	W501	Schmitt Trigger										
	W500	Comparator										
	S181	part same										
	W305	part same										

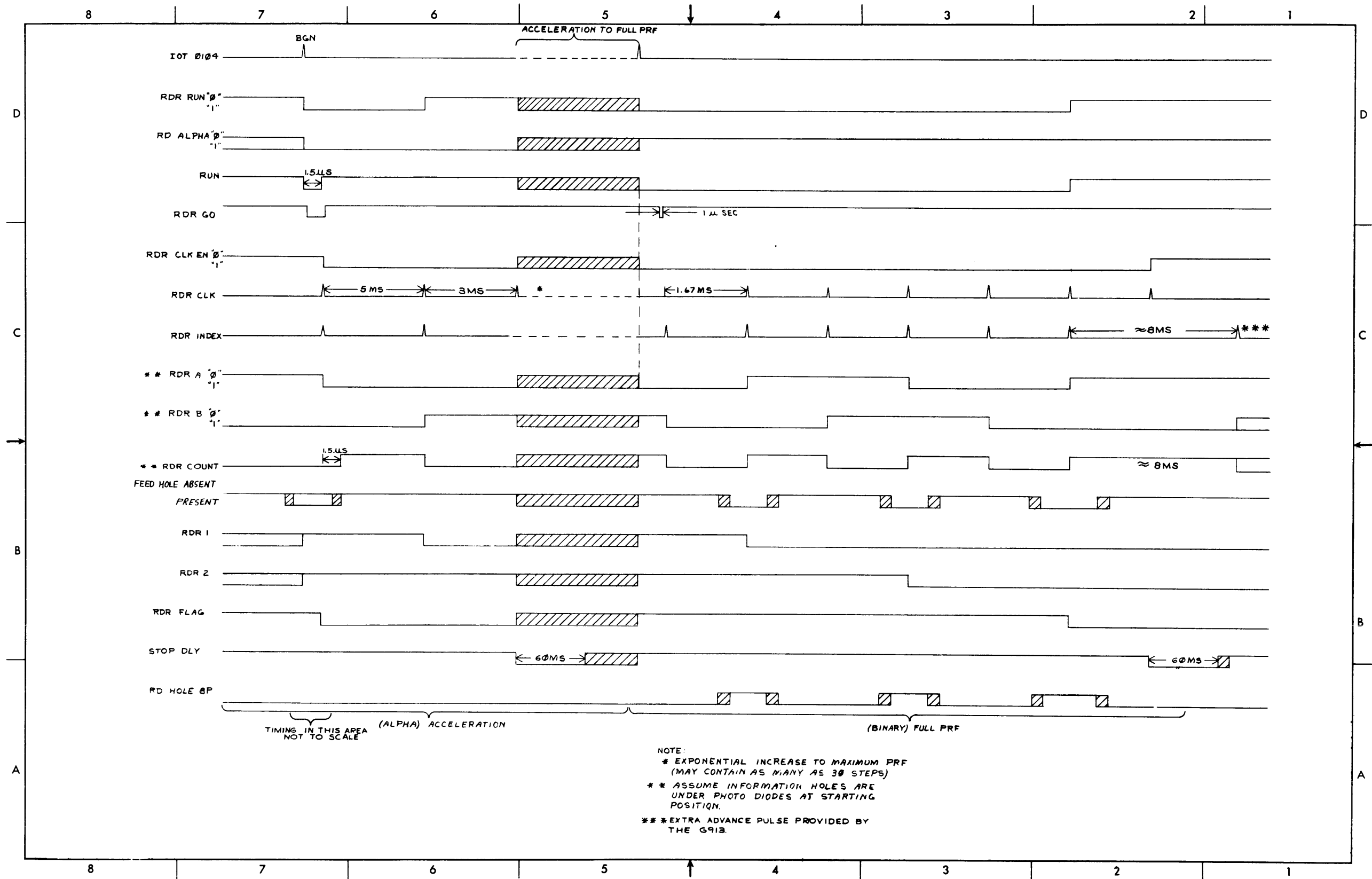
A-PL-KD09-C-14 PDP-9/L IO Module List

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COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
CAPACITOR	2.2 MFD	-	C25H	C25J	+
RESISTOR	2.7K 5% 1/4W		C25J	C25L	
CAPACITOR	0.01 MFD	-	D25E	D25C	+
RESISTOR	4.7K 10% 1/4W		D26K	D26B	
RESISTOR	10K 1/4W 10%		A21T	B21B	
CAPACITOR	175MFD 10%	-	C27J	C27C	+
RESISTOR	20K 1/4W 5%		C27P	C27S	
CAPACITOR	39 MFD 10%	-	C25R	C25S	+
RESISTOR	24K 1/4W 5%		C25S	C25U	
CAPACITOR	0.02 MFD 50V	-	A24H	A24J	+
RESISTOR	3K 1/4W 5%		F05J	F05L	
RESISTOR	1.5K 1/4W		A17V	B17B	
RESISTOR	1K 1/4W 10%		A24J	A24L	
RESISTOR	3K 1/4W 5%		D21P	D21B	
CAPACITOR	6.8 MFD	-	E12M	E12C	+
CAPACITOR	270 PF 5%		E40J	E40K	
RESISTOR	3.3K 1/4W 5%		E05S	E05U	
RESISTOR	3.3K 1/4W 5%		E05J	E05L	
*PRE API SYNC	JUMPER		J10S	J10C	
**34 DISPLAY	JUMPER		F40T	F40C	
***WIRE JUMPER			A32P	A28P	
**** CLK SYNC (I) JUMPER			F08C	F08U	
*REMOVE JUMPER WHEN API IS INSTALLED					
**REMOVE JUMPER WHEN 34 DISPLAY IS INSTALLED					
***REMOVE JUMPER WHEN ME09 IS INSTALLED					
**** REMOVE JUMPER WHEN KW09-L IS INSTALLED					

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A-CP-KD09-C-16 External Component List I/O PDP-9/L



D-TD-KD09-C-17 Reader Timing Diagram Alpha and Binary Mode

8			7			6			5			4			3			2			1					
SIGNAL NAME			ORIGIN			DESTINATION			SIGNAL NAME			ORIGIN			DESTINATION			SIGNAL NAME			ORIGIN			DESTINATION		
AC RD	3-3					DEI	4-1	3-1	IOT(1)B	9-1	3-3, 3-2, 7-1	RDR COUNT	9-1													
ACT API GR	KF 1-1					DLY	3-3	3-2	IOT 0002	3-1	3-2, 12-2	RDR FEED	9-1													
ACT PI	KF 1-1					DONE	4-1	3-2, 3-3	IOT 0004	9-1	7-1, 12-1, 3-3	RDR FLG	9-1													
ADDR SW(03-17)	6-1	7-1, 7-2				DPY D	4-1	7-1	IOT 0102	9-1																
ADSO	4-1					DPY R	4-1		IOT 0104	7-1																
ADSO(G)	7-1					DPY ON BUS	34H 1-2	KF 1-4, 34H, 1-1	IOT 0204	10-1	7-1, 12-1, 3-3	RDR FLG(B)	9-1													
AM SYNC BUS(B)	4-1					DS 0	3-1	KF 1-3, 2-1	IOT 0302	11-1		RDR GD	9-1													
API D	4-1					DS 0 P	3-1		IOT 0404	11-2		RDR INDEK	9-1													
API BK RO	KF 1-3					DS 1	3-1	2-1, KF 1-1	IOT 0502	34H 1-2	34H 1-1	RDR NO TAPE	9-1													
API BK RO 1(B)	KF 1-1					DS 1 P	3-1	KF 1-3	IOT 0602	34H 1-2	34H 1-1	RDR ON BUS	7-1													
API ENABLE	KF 1-3					DS 2	3-1	2-1, KF 1-3, 1+1	IOT 0704	34H 1-2	34H 1-1	RDR PWR	9-1													
API IO CLR	KF 1-3					DS 3	3-1	2-1, 11-2, KF 1-3, 34H 1-2	IOT 0804	34H 1-2	34H 1-1	RDR RUN	9-1													
API IO CLR	3-2					DS 3 P	3-1	9-1, 11-1, 10-1, 34H 1-1	IOT 0904	3-1	34H 1-1	RDR SEL(B)	9-1													
API ON BUS	7-1	7-2				DS 4	3-1	KF 1-1	IOT 5502	KF 1-3	7-1, 12-2, 3-3	RDR 1	9-1													
API SEL	KF 1-3					DS 4 P	3-1	11-1, 10-1, 2-1, KF 1-1, 34H 1-2	IOT 5504	KF 1-3	KF 1-4, KF 1-1	RDR 2	9-1													
API STRG	KF 1-3					DS 5	3-1	1-1, 34H 1-2	IRI	4-1	3-3	RDR D	4-1													
API SYNC	KF 1-1	12-2				DS 5 P	3-1	11-2, 8-1, KF 1-3	KBD IO CA INH	11-1	12-1, 7-1, 9-1	READ IN 1	8-1													
API SYNC RQ	KF 1-1					EAE	4-1	34H 1-2	KBD SEL	11-1		READ IN 2	8-1													
API 0 EN	KF 1-4	2-2				EXIT	4-1	2-1, 11-1, 9-1, KF 1-3, 34H 1-2	KBD SEL(B)	11-1		RI 1(B)	8-1													
API 0 EN OUT	2-2					FEED HOLE	4-2	10-1, 11-2, KF 1-1, 34H 1-2	KDPW	4-1	6-1	RI 2(1)B	8-1													
API 0 GR	KF 1-3, 1-4	2-2				FWD FD AND NDX	10-1		KEY PLY	4-1	8-1	RPI(1-7)EN	KF 1-1													
API 0 RO	KF 1-4, 1-1	2-2				H IO	3-1		KID	4-1	9-1	RQ SYNC(9-7)	KF 1-1													
API 0 RO(B)	KF 1-1, 1-2					IN LAST UNIT	11-1		KMT	6-1	4-1	RQ 00 EN	KF 1-2													
API 0 RO NEG	KF 1-1	7-1				INC MB	3-3		KRI	4-1	4-1	RQ 01 EN	KF 1-1													
API(4-7)RO	KF 1-1	KF 1-2, 7-1, 7-2, 12-2				INC + DCH	3-2		KXOM	6-1	4-1	RQ 02 EN	KF 1-2													
API 1 EN	KF 14					INPUT IO RESTART	3-3		LOCK	6-1	KF 1-1, 3-2, 4-1	RSB	8-1													
API 1 GR	KF 1-4					INPUT IO RESTART	8-1		LP OUT	34H 1-1		RT CLK	8-1													
API 1 RO	KF 1-4					INT RD RO BUS	3-3		LP STB	34H 1-1		RUN	9-1													
API 1 RO(B)	KF 1-1					*INT SKP RO BUS	12-1		MB(00-17)	4-1	6-1, 3-1, 3-3	SD 0	3-1													
API 1 RO NEG	KF 1-4					INTENSITY	34H 1-1		NR	4-1		SD 0 P	3-1													
API 2 EN	KF 1-4					IO ADDR D	4-1		PFIO	4-1		SD 1	3-1													
API 2 GR	KF 1-3					IO ADDR ON BUS	7-1		PF API RQ(1)	KF 1-4		SEL 1 P	3-1													
API 2 RO	KF 1-4					IO ADDR(03-17)	2-2		PJ DISABLE	KF 1-3		SEL(B-2)	KF 1-4													
API 2 RO(B)	KF 1-1					IO ADDR(12, 14, 16, 17)	KF 1-4		PIE	3-2		SEN(1)B	4-1													
API 2 RO NEG	KF 1-2					IO ADDR(03-05, 16, 17)	5-1		PL(00-02)EN	KF 1-1		SKIP RO	2-1													
API 3 RO	KF 1-1					IO ADDR(06-15)B	5-1		PL 00 EN P	KF 1-1		STATUS ON BUS	7-1													
API 3 RO(B)	KF 1-2					IO BUS(00-17)B	4-1		PLS CONTROL 0	KF 1-4		STATUS D	4-1													
API 3 RO NEG	KF 1-1					IO CLK POS	3-2		PRE API SYNC	KF 1-1		STOP DLY	4-1													
API(4-7)RO(1)B	KF 1-2					IO CLK(B)	3-3		PRG API AVNC EN	KF 1-1		SW CLK	4-1													
AUTO RESTART	KF 1-1					IO CLR(B)	3-2		*PRG INT RO	2-1	9-2, 10-1, 11-1, 34H 1-1, 1-1, KF 1-1, 3-2, 11-2	TAPE	10-1													
BK SYNC	3-2					IO CLR(B)	3-2		PROG SY	3-2		T-PRINTER FLG	11-2													
BK 0	3-3					IO CLR(B)	3-3		PROG SY(1)B	3-2		T-PRINTER SEL(B)	11-2													
BK 0(B)	3-3					IO CLR(B)	3-2		PROG SYNC	3-2		TT IN ACT	11-1													
BK 0(1)B	3-3					IO CLR(B)	3-2		PTR API RO	KF 1-4		TT KBD IN	11-1													
BK 1	3-3					IO CLR(B)	3-2		PTR GR	KF 1-4		TT LINE	11-2													
BK 1(B)	3-3					IO CLR(B)	3-2		PUN	10-1		TT OUT ACT	11-1													
BR 0	34H 1-1					IO CLR(B)	3-2		PUN FEED	10-1		TT RDR RUN	11-1													
BR 1	34H 1-1					IO CLR(B)	3-2		PUN FLG	10-1		TT SYNC	11-1													
CAF EN	3-1					IO CLR(B)	3-2		PUN HOLE(1-0)	10-1		TTI CLK	11-1													
CAF EN(B)	3-1					IO CLR(B)	3-2		PUN LINE	10-1		TTI FULL	11-1													
CAL	4-1					IO CLR(B)	3-2		PUN NO TAPE	10-1		TTI INITIALIZE	11-1													
CLK	4-1					IO CLR(B)	3-2		PUN PWR	10-1		TTI LOAD	11-1													
CLK DLY D	3-3					IO CLR(B)	3-2		PUN PWR ON	10-1		TTI ON BUS	7-1													
CLK EN	3-2					IO CLR(B)	3-2		PUN SEL	10-1		TTI(0-7)	11-1													
CLK FLG	3-2					IO CLR(B)	3-2		PUN SPD	10-1		TTI D	4-1													
CLK POS	4-1					IO CLR(B)	3-2		PUN SYNC	10-1		TTO CLK	11-2													
CLK RQ	2-2					IO CLR(B)	3-2		PV	4-1		TTO EN	11-2													
CLK SYNC	3-2					IO CLR(B)	3-2		PWR CLR POS	KF 1-1		TTO EO 0	11-2													
CLK(B)	3-2					IO CLR(B)	3-2		PWR ON	KF 1-1		TTO LOAD	11-2													
CLR API GR	KF 7-3					IO CLR(B)	3-2		PWR(0)	9-1		TTO START	11-2													
CLR API GR	KF 1-1					IO CLR(B)	3-2		RB(00-17)	9-2		TTO STOP	11-2													
CLR RUN	10-1					IO CLR(B)	3-2		RD HOLE(1-0)	9-2		TTO(0-7)	11-2													
CLR RDR	9-1					IO CLR(B)	3-2		RD HOLE(1-0)B	9-2		UM	4-1													
CDV API RO	KF 1-4					IO CLR(B)	3-2		RD HOLE 7(B)	9-2		UM(0)B	3-3													
DASO	4-1					IO CLR(B)	3-2		RD HOLE 7(C)	9-2																